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MICROCOMPUTER MN102L00

MN102L59D/59C/F59D

LSI User's Manual

Pub.No.22259-010E

Panasonic

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About This Manual

This manual is intended for assembly-language programming engineers. It describes the internal configuration and hardware functions of the MN102L59x series microcontrollers.

Text Conventions

This manual contains titles, sub-titles, special notes and warnings. Supplementary comments appear in the sidebar.

Key Information
This note describes key points of an operation.

Warning
Please read and follow these instructions to prevent damage or reduced performance.

Finding Desired Information

This manual provides four methods for finding desired information quickly and easily.

(1) An index for the front of the manual for finding each section.

(2) A table of contents at the front of the manual for finding desired titles.

(3) Lists of figures and tables at the front of the manual for finding illustrations and charts by names.

(4) A chapter name is located at the upper corner of each page.

Related Manuals

- MN10200 Series Linear Addressing Version LSI User Manual (Describes the MN10200 series specifications)
- MN10200 Series Linear Addressing Version Instruction Manual (Describes the instruction set)
- MN10200 Series Linear Addressing Version C Compiler User Manual Usage Guide (Describes the installation, commands, and options for the C complier)
- MN10200 Series Linear Addressing Version C Compiler User Manual Language Description (Describes the syntax for the C complier)
- MN10200 Series Linear Addressing Version C Compiler User Manual Library Reference (Describes the standard libraries for the C complier)
- MN10200 Series Linear Addressing Version Cross Assembler User Manual Language Description (Describes the assembler syntax and notation)
- MN10200 Series Linear Addressing Version C Source Code Debugger User Manual (Describes the use of the C source code debugger)
- MN10200 Series Linear Addressing Version PanaXSeries Installation Manual (Describes the installation of the C complier, cross-assembler, and C source code debugger and the procedures for using the in-circuit emulator)

Questions and Comments

Please send your questions, comments and suggestions to your local semiconductor design center. See the last page of this manual for a list of addresses and telephone numbers.

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Chapter 1 Overview

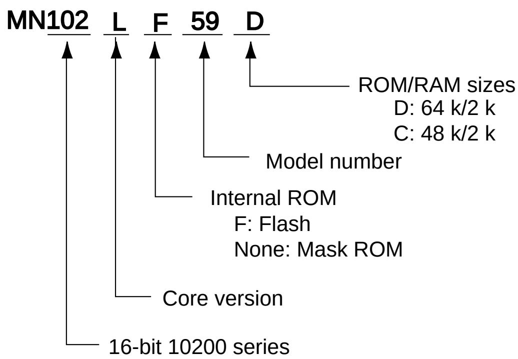
1-1 Overview

1-1-1 Introduction

The MN10200 series linear addressing version designs the new architecture for C-language programming based on a detailed analysis for embedded applications. This improves the system architecture in speed and function to meet the requirements in user systems including miniaturization and low power consumption.

The 16-bit MN102L (F) 59x series has three-phase inverter control function, which realizes high-efficiency real-time control in motor control.
This series adapts a load/store architecture method for computing within registers and a harvard architecture method for separating instructions bus and operand bus. Using one byte/one machine cycle basic instructions minimizes code size and improves compiler efficiency.

[Model Explanation]



1-1-2 Features

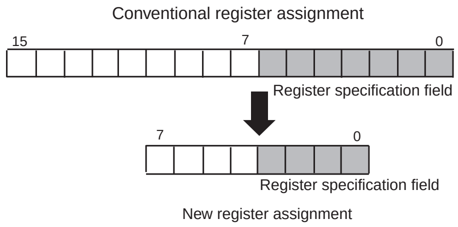
This series contains a flexible and optimized hardware architecture as well as a simple and efficient instruction set. It obtains economical efficiency and high speed. This section describes the features of this series CPU.

1. Linear Addressing for Large Systems

The MN10200 series contains up to 16 Mbytes of linear address space. The CPU provides an effective development environment without detecting borders between address spaces. The hardware architecture is also optimized for large systems. The memory is not divided into instruction space and data space so that operations can share instructions.

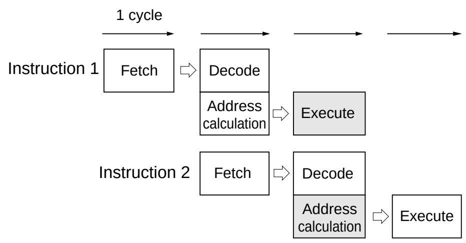
2. Single-byte Basic Instruction Length

The MN10200 series has replaced general registers with eight internal CPU registers divided four address registers (A0 to A3) and four data registers (D0 to D3). The register specification fields are four bits or less, and the code sizes of the frequently used basic instructions including register- to-register operations and load/store operations are one byte.



3. High-speed Pipeline Processing

The MN10200 series executes instructions in a 3-stage pipeline: fetch, decode and execute. This allows the MN10200 series to execute instructions of single byte in one machine cycle.

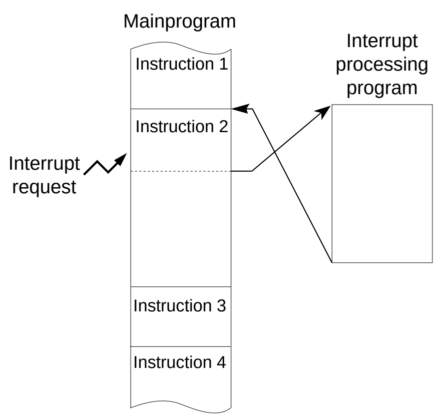


4. Simple Instruction Set

The MN10200 series uses an instruction set of 36 instructions, designed specially for the programming model for embedded applications. To compress the code size, instructions have a variable length of one byte to five bytes. The most frequently used instructions in C-language compiler are single byte.

5. High-speed Interrupt Response

The MN10200 series can respond quickly to interrupt handling even during the execution of the instruction with long execution cycles by suspending it. After an interrupt occurs, the program moves to the interrupt handler within 11 cycles or less. The MN10200 series enhances real-time control performance using the interrupt handler which adjusts interrupt handling speed depending on user requirements.



6. Flexible Interrupt Control Structure

The interrupt controller is divided into eight groups (Group 0 is reserved for NMI.) and supports a maximum of four vectors for each group in total of 24 vectors. Each group can be set to one of seven priority levels. This provides the software design flexibility and accurate control. The CPU is compatible with software from previous Panasonic peripheral modules.

7. C-Language Development Environment

The MN10200 series contains highly efficient C compiler and simple hardware optimized for C-language programming. With this advantage, this series improves development environment for C-language embedded applications without expanding the program size. The **PanaXSeries** development tools support the MN10200 series devices.

8. Outstanding Power Savings

The MN10200 series contains separate buses which distribute and reduce load capacitance. This greatly reduces overall power consumption compared to our conventional models. The MN10200 series also supports two modes of HALT and STOP for power savings.

1-1-3 Overview

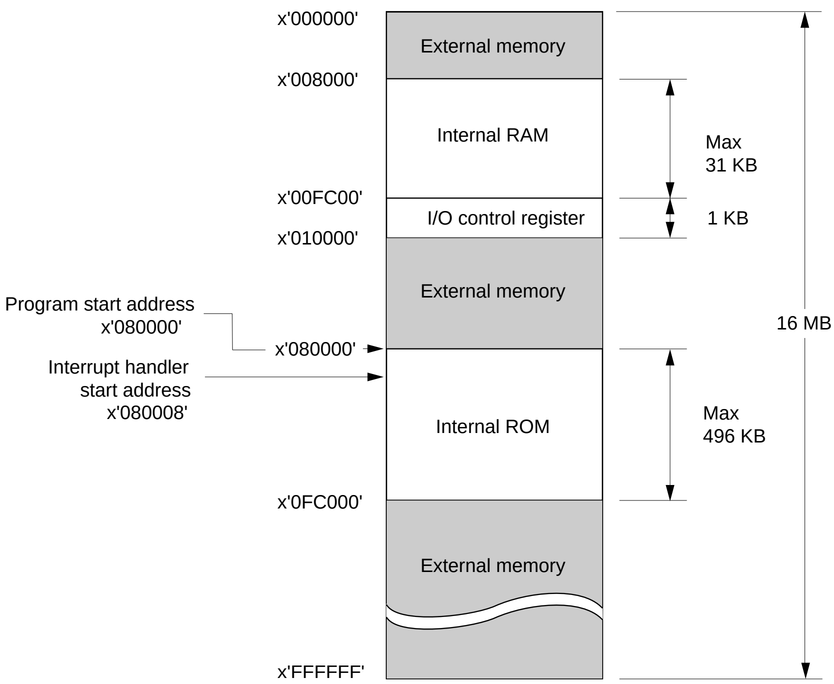
This section describes the basic configuration and function of this series.

■ Address Space

The memory contains up to 16-Mbyte linear address space. The instruction space and data space are not separated so that internal RAM and special function registers for internal peripheral functions are allocated into the first 64 KB in memory as the basic configuration.

This is a general example of the memory expansion mode.

Both the start address and the end address of internal RAM are changed within x"008000" to x"00FBFF" depending on models.



The start address of internal ROM is fixed at x"080000" while the end address of internal ROM is changed depending on sizes of internal ROM. (The end address in this example is 496 KB.)

Figure 1-1-1 Address Space

Table 1-1-1 Memory Modes

Mode	Address bit width	Internal ROM capacity
single chip mode	Up to 24 bits	16 KB or more

External memory area can not be used in this series. Please refer to Chapter 2.

■ Internal Registers, Memory and Special Function Registers

Program Counter

23 … 0
PC

The program counter specifies the address (24 bits) of the program during the execution.

Address Registers

23 … 0
A0
A1
A2
A3

The address registers specify the data location on the memory. A3 is assigned as the stack pointer.

Data Registers

23 … 0
D0
D1
D2
D3

The data registers perform all arithmetic and logic operations. When the byte (8-bit) data or the word (16-bit) data is transferred to memory or another register, the instruction adds a zero or a sign extension.

Multiplication/Division Register

15 … 0
MDR

The multiplication/division register stores the upper 16 bits of the 32-bit product of the multiplication operations. In division operations, this register stores the upper 16 bits of the 32-bit dividend before the execution and the 16-bit remainder of the quotient after the execution.

Processor Status Word

15 … 0
PSW

The processor status word indicates the CPU status. This register stores the operation result flags and interrupt mask levels.

Memory, Special Registers, I/O Ports

Memory (ROM and RAM), special registers for controlling peripheral functions and I/O ports are assigned to the same address space.

ROM	
RAM	
CPUM, MEMCTR, IAGR	Internal Control Registers
SYSCTL	System Control Registers
GnICR, EXTMD, NFCTR, ...	Interrupt Control Registers
SCnMD0, SCnMD1, SCnMD2, ...	Serial Interface
ANCTR, ANBUF	A/D Converter
TMnMD, TMnBC, TMnBR, ...	Timers/Counters
PnMD, PnDIR, PnOUT, ...	I/O Ports

■ Interrupt Controller

The interrupt controller (group 0 to group 7) allocated to the outside of the CPU controls all nonmaskable interrupts and maskable interrupts except reset. Each group contains up to four interrupt vectors and specifies any of seven priority levels.

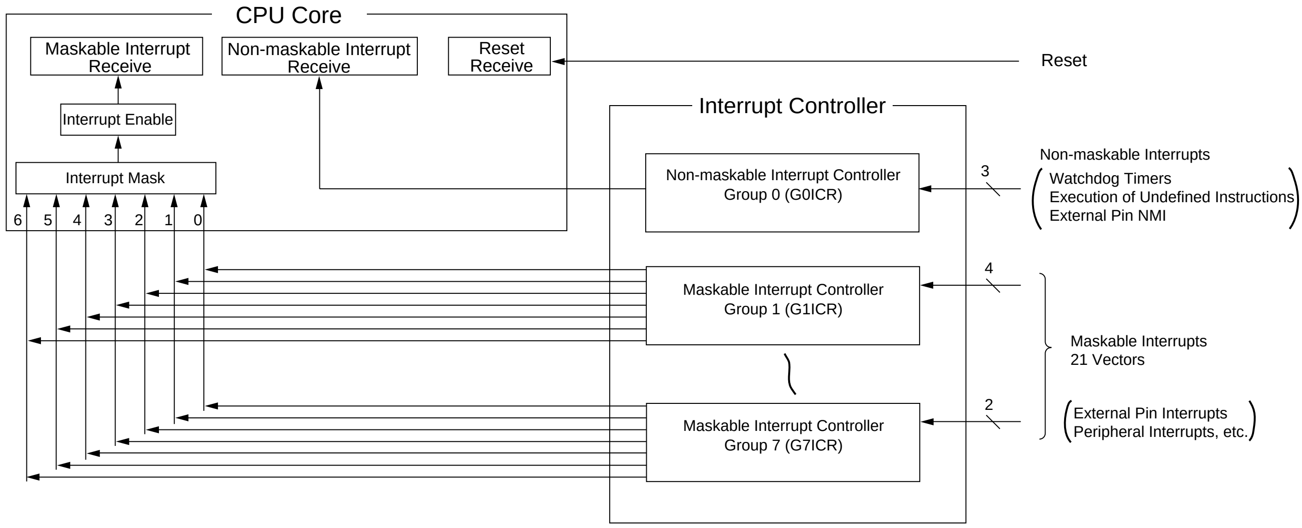


Figure 1-1-2 Interrupt Controller Configuration

The CPU checks the processor status word to determine whether an interrupt request is accepted or not. When an interrupt is accepted, automatic servicing by hardware starts and the program counter and PSW are pushed to the stack. Next, the program moves to the interrupt. After specifying the interrupt vector, it branches to the entry address of the interrupt service for that interrupt.

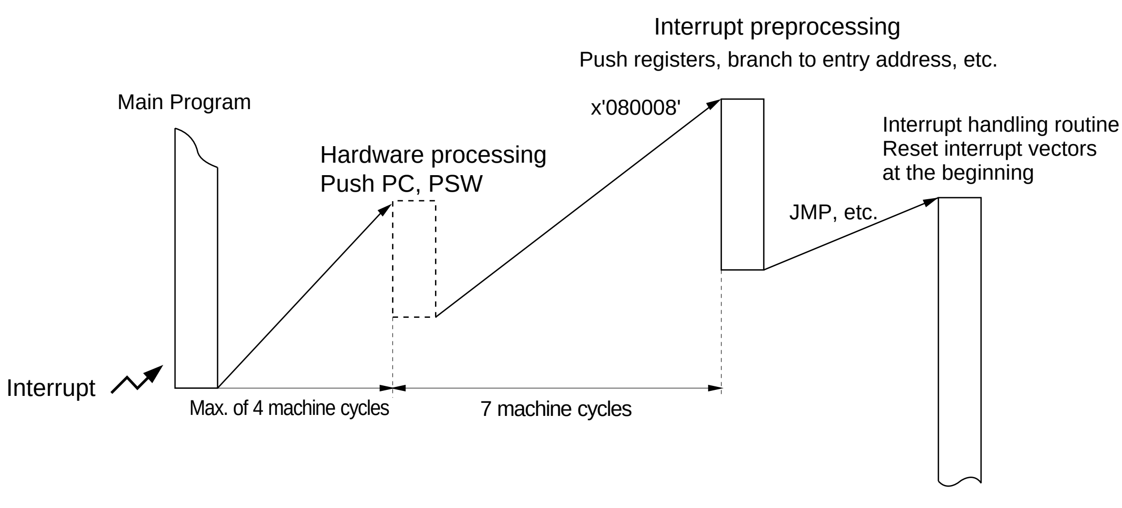


Figure 1-1-3 Interrupt Servicing Sequence

1-2 Basic Specifications

This section describes the basic specification of this series. Please refer to Product Standards for details.

Table 1-2-1 Basic Specifications (1/2)

CPU Structure	Load/store architecture Eight registers: Four 24-bit data registers Four 24-bit address registers Others : 24-bit program counter 16-bit processor status word 16-bit multiplication/division register
Instruction	36 instructions 6 addressing modes One-byte primitive instruction length Code assignment: 1 to 2 bytes (Basic) + 0 to 3 bytes (Extension)
Basic Performance	10 MHz internal operating frequency with a 5-MHz oscillator and internal 4x-speed Clock cycles: For instruction execution, minimum 1 cycle (100 ns) For register-to-register operations, minimum 1 cycle For load/store operations, minimum 1 cycle For conditional branching operations, 1 to 3 cycles
Pipeline	3 stages: Instruction fetch, decode, execute
Address Space	16-MB linear address space
Low-power Mode	STOP mode, HALT mode
Frequency Circuit	Outside: Up to 5 MHz (Inside 20 MHz : Internal 4x-speed)
Interrupt	24 vectors 3 non-maskable interrupts 21 maskable interrupts (7 interrupt priority level settings) 7 external interrupts 6 external interrupts (individual IRQ, edge specification) 1 external non-maskable interrupt 17 internal interrupts 12 timer interrupts, 2 serial interrupts, 1 A/D interrupt, 1 watchdog timer interrupt, 1 undefined instruction interrupt

Table 1-2-1 Basic Specifications (2/2)

Timer/Counter	Nine 8-bit timers Reload timer Cascading function Timer output (duty of 1:1) Internal clock source or external clock source Serial interface clock generation Start timing generation for A/D converter Output 2 channels simplified PWM Output 1 channel simplified 6-phase PWM Three 16-bit timers Compare registers Internal clock source or external clock source Timer output (duty of 1:1) PWM 1 channel high-efficiency inverter control (output 6-phase PWM) 17-bit watchdog timer
Serial Interface	2 half duplex UART/synchronous (shared) serial interfaces
Analog Interface	A/D converter Twelve 10-bit inputs (4 channels are shared.) Auto scanning (0 to 7 channel settings)
I/O Port	52 I/O ports (All shared pins)
Package	64-pin LQFP pitch: 0.8 mm dimension: 14-mm-square

1-3 Block Diagram

Figure 1-3-1 shows the block diagram including the CPU core and Table 1-3-1 describes the block functions.

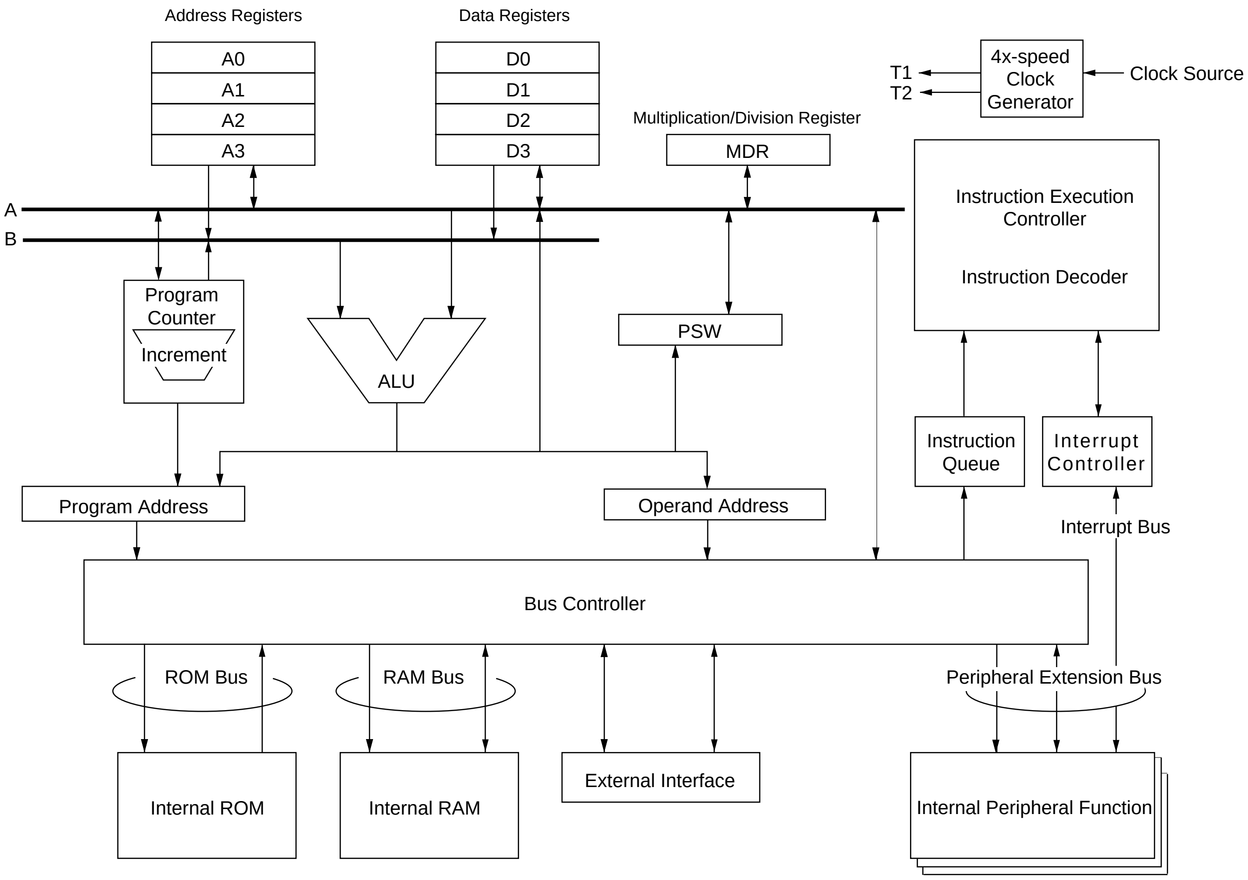


Figure 1-3-1 Block Diagram

Table 1-3-1 Block Functions

Block	Functions
Clock Generator	The clock generator contains the clock oscillation circuit connected to an external crystal and supplies the clock to all CPU blocks. (It has a built-in 4x-speed circuit.)
Program Counter	The program counter generates addresses for instruction queues. Normally, it gets increments based on the sequencer indication, but for branch instructions and interrupt acceptance, it sets the branch address or ALU operation results.
Instruction Queue	The instruction queue saves up to 4 bytes of prefetched instructions.
Instruction Decoder	The instruction decoder decodes the instruction queue content, generates control signals needed for the instruction execution, and executes the instruction by controlling each block in the CPU.
Instruction Execution Controller	The instruction execution controller controls the operations of each CPU function based on results from the instruction decoder and interrupt requests.
ALU	The ALU calculates the operand addresses for arithmetic operations, logic operations, shift operations, register relative indirect, indexed addressing and register indirect addressing mode.
Internal ROM, Internal RAM	Internal ROM and internal RAM are allocated as the execution program, data and stack areas.
Address Registers (An)	The address registers (An) store the addresses of memory accessed during data transfer. They also store the base addresses in the register relative indirect, indexed addressing and register indirect addressing mode.
Operation Registers (Dn, MDR)	The data registers (Dn) store the operation results and transfer the data to memory. They also store the offset addresses in indexed addressing and register indirect addressing mode. The multiplication/division register (MDR) stores the data for multiplication/division operations.
PSW	The processor status word (PSW) stores the flags that indicate the status of the CPU interrupt controller and operation results.
Interrupt Controller	The interrupt controller detects the interrupt requests from the peripheral functions, and requests the CPU to move to the interrupt handling.
Bus Controller	The bus controller controls the connection between the CPU internal bus and the CPU external bus. It also contains the bus arbitration function.
Internal Peripheral Function	This series contains the peripheral functions including timers, serial interface, A/D converter and so on.

1-4 Pin Description

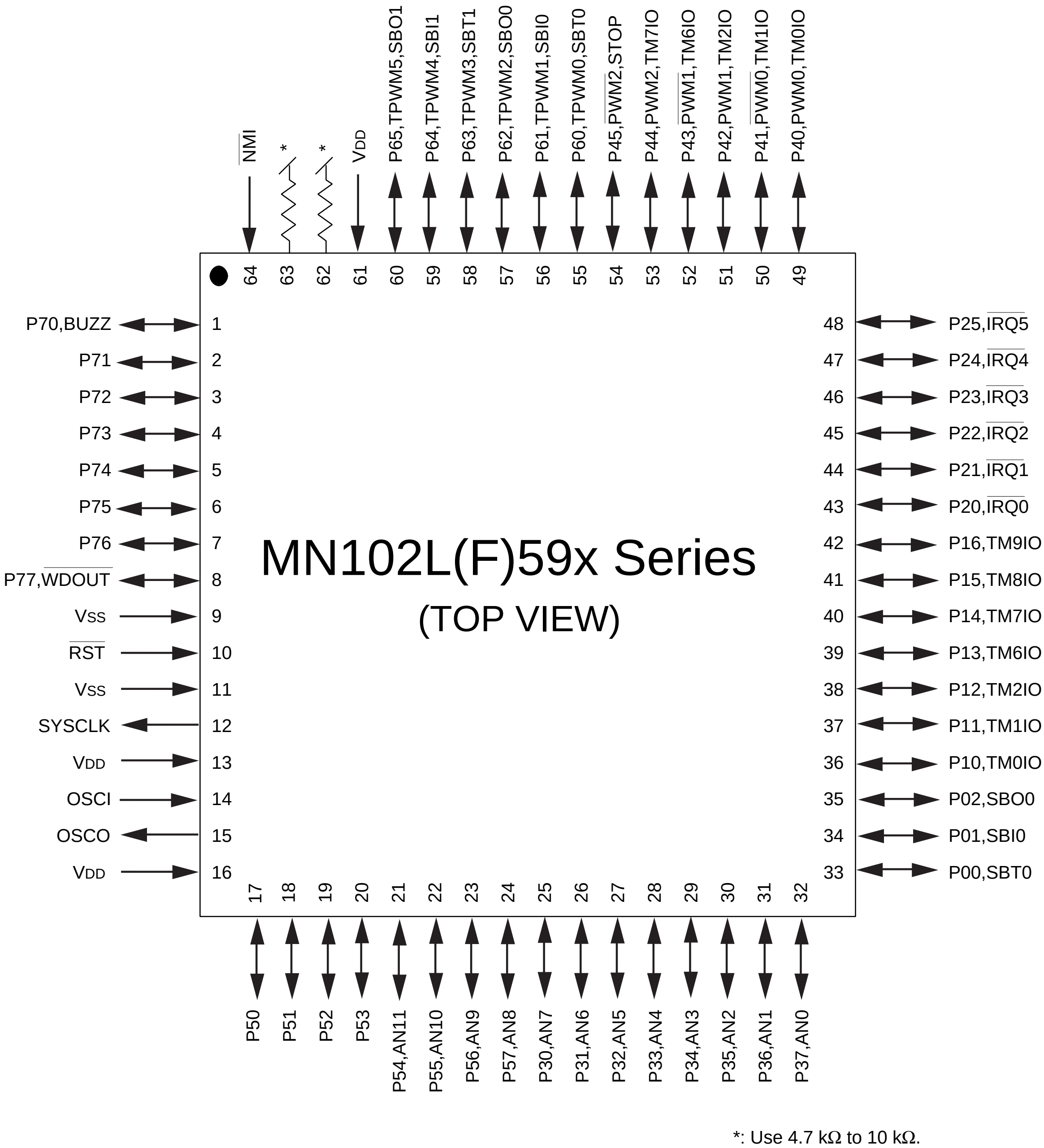


Figure 1-4-1 Pin Configuration

The unused input pins are connected to VDD/VSS, the unused output pins are opened and the unused I/O pins are connected to VDD/VSS by setting the direction in ports or opened.

1-4-1 List of Pin Functions

Refer to “8-2-3 List of Pin Functions” for each pin’s input level, and Schmitt and pull-up resistor availability. TTL in the input level column means that the input is determined at TTL level. CMOS in the input level column means that the input is determined at CMOS level. The column with “yes” sign shows Schmitt, while the column with no mark shows no Schmidt. Pull-up and pull-down resistors are in the column with “yes”. The column with “programmable” can be set by pull-up and puill-down control registers (PPUP, PPDW). Please see “Chapter 7 Ports” for details.

Table 1-4-1 List of Pin Functions (1/4)

Pin Name	Input/Output	Shared Pin	Function	Description
V_{DD}	—	—	Power	There are three V_{DD} pins. Connect these three pins to a power supply of 4.5 V to 5.5 V.
V_{SS}	—	—	Power (Ground)	There are two V_{SS} pins. Connect these two pins to a power supply of 0 V.
OSCI OSCO	Input Output	— —	High-speed Oscillator Input (Max: 5 MHz) High-speed Oscillator Output (Max: 5 MHz)	For a self-excited oscillator configuration, connect crystal or ceramic oscillator across these two pins. They have a built-in feedback resistor between them. For stability, insert capacitor of 20 pF to 33 pF between the OSCI or OSCO pin and V_{SS} pin. (For the exact capacitance, consult the oscillator manufacturer.) [☞ Figure 1-4-2 OSCI and OSCO Connection Example] For an external oscillator configuration, connect the OSCI pin to an oscillator with an amplitude of maximum 5 MHz at the width between V_{DD} and V_{SS}. Leave the OSCO open. Connecting the OSCO pin with the external circuit is not allowed. Select the SYSCLK pin as a synchronous signal.
$\overline{RST}$	Input	—	Reset Input	This pin resets the chip. With a 5-MHz oscillator, reset starts when the low level is input to this pin for more than 200 ns. Reset may start even when the noise is input to this pin for less than 200 ns, so please pay highly attention to noise. Reset is released when the high level is input to the pin. The oscillation waits of the high-speed oscillation pin (OSCI) are performed (approximately 6 ms to 7 ms with a 5-MHz oscillator). After that, the chip starts executing the instruction from x”080000”. [☞ Figure 1-4-3 Reset Connection Example]

Table 1-4-1 List of Pin Functions (2/4)

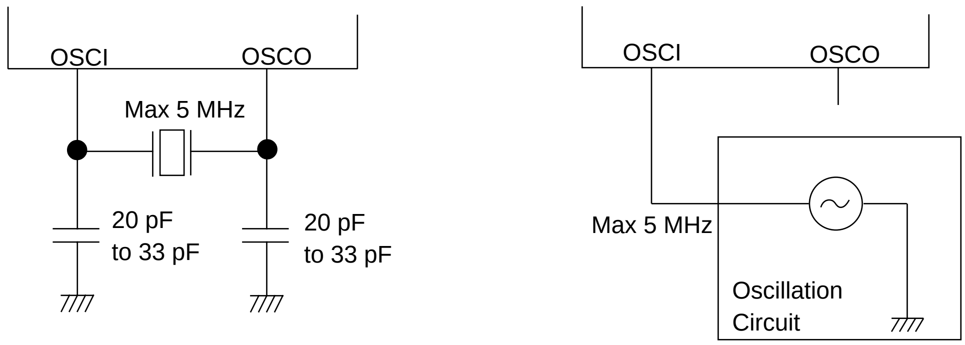
Pin Name	Input/Output	Shared Pin	Function	Description
SYSCLK	Output	—	System Clock Output	This pin provides the system clock. After reset release, the oscillation waits of OSCI are always performed and this pin outputs the clock of 10 MHz at a 5-MHz oscillation. Please keep in mind that this pin holds the high level until the oscillation waits are released after the $\overline{\text{RST}}$ pin becomes the low level.
P70	I/O	—	General-purpose Port 7	This pin can be used as a general-purpose input/output port. [Chapter 7 Ports]
	Output	BUZZ	Buzzer Output	This pis outputs the square wave that divides $1/2^{11}$ to $1/2^{14}$ of system clock. [Chapter 4 Timers]
P76 to P71	I/O	—	General-purpose Port 7	These pins can be used as general-purpose input/output ports. [Chapter 7 Ports]
P77	I/O		General-purpose Port 7	This pin can be used as a general-purpose input/output port. [Chapter 7 Ports]
	Output	$\overline{\text{WDOUT}}$	Watchdog Timer Overflow Signal	When the watchdog timer is overflowed, pulse is output.
P53 to P50	I/O		General-purpose Port 5	When these pins are used as general-purpose input/output ports, input/output direction control is bit-oriented. [Chapter 7 Ports]
P57 to P54	I/O		General-purpose Port 5	When these pins are used as general-purpose input/output ports, input/output direction control is bit-oriented.
	Input	AN11 to AN8	A/D Converter Input	These are input pins for A/D converter. [Chapter 6 Analog interface]
P37 to P30	I/O		General-purpose Port 3	When these pins are used as general-purpose input/output ports, input/output direction control is bit-oriented.
	Input	AN7 to AN0	A/D Converter Input	These are input pins for A/D converter. [Chapter 6 Analog interface]

Table 1-4-1 List of Pin Functions (3/4)

Pin Name	Input/Output	Shared Pin	Function	Description
P00	I/O I/O	 SBT0	General-purpose Port 0 Serial Interface 0 Clock Input/Output	When this pin is used as a general-purpose input/output port, input/output direction control is bit-oriented. [Chapter 7 Ports] These pins can be used as synchronous transfer clock signals, data input and data input/output for serial interface. When these are unused, the input pins are fixed as high level while the output pins are opened. [Chapter 5 Serial Interface]
P01	I/O Input	 SBI0	General-purpose Port 0 Serial Interface 0 Data Input	
P02	I/O I/O	 SBO0	General-purpose Port 0 Serial Interface 0 Data Input/Output	
P16 to P10	I/O		General-purpose Port 1	When these pins are used as general-purpose input/output ports, input/output direction control is bit-oriented. [Chapter 7 Ports]
	I/O	TM9IO to TM6IO	Timer 9 to Timer 6 Input/Output	These pins are timer 9 to timer 6 input/output pins.
		TM2IO to TM0IO	Timer 2 to Timer 0 Input/Output	These pins are timer 2 to timer 0 input/output pins. [Chapter 4 Timers]
P25 to P20	I/O		General-purpose Port 2	When these pins are used as general-purpose input/output ports, input/output direction control is bit-oriented. [Chapter 7 Ports]
	Input	$\overline{IRQ5}$ to $\overline{IRQ0}$	External Interrupt	

Table 1-4-1 List of Pin Functions (4/4)

Pin Name	Input/Output	Shared Pin	Function	Description
P45 to P40	I/O		General-purpose Port 4	When these pins are used as general-purpose input/output ports, input/output direction control is bit-oriented. [Chapter 7 Ports]
	Output	STOP	STOP Status Signal	These pins become high level during STOP or HOLT mode.
	Output	PWM2 to PWM0 $\overline{\text{PWM2}}$ to $\overline{\text{PWM0}}$	Timer 11 Output	These are output pins of timer 11 (6-phase PWM wave form).
	I/O	TM7IO, TM6IO	Timer 7 and 6 Input/Output	These are input/output pins of timer 7 and timer 6.
		TM2IO to TM0IO	Timer 2 to 0 Input/Output	These are input/output pins of timer 2 to 0. [Chapter 4 Timers]
P65 to P60	I/O		General-purpose Port 6	When these pins are used as general-purpose input/output ports, input/output direction control is bit-oriented. [Chapter 7 Ports]
	Output	TPWM5 to TPWM0	Timer 10 Output	These are output pins of timer 10 (Simplified 6-phase PWM waveform). [Chapter 4 Timers]
	I/O	SBT1 to 0	Serial Interface Clock Input/Output	These pins can be used as synchronous transfer clock signal, data input and data output for serial interface. When these are unused, the input pins are fixed as high level while the output pins are opened. [Chapter 5 Serial interface]
	Input	SBT1 to 0	Serial Interface Data Input/Output	
	Output	SBO1 to 0	Serial Interface Data Output	
NMI	Input		$\overline{\text{NMI}}$	An $\overline{\text{NMI}}$ interrupt occurs on the falling edge to low level at negative logic. (<u>When reading the Port 2, the pin value can be monitored at bit 6.</u>)



(Note)Capacity varies acoording to crystal oscillator.

Figure 1-4-2 OSCI and OSCO Connection Example

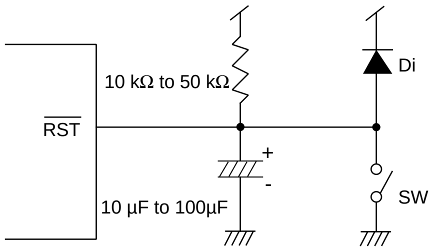
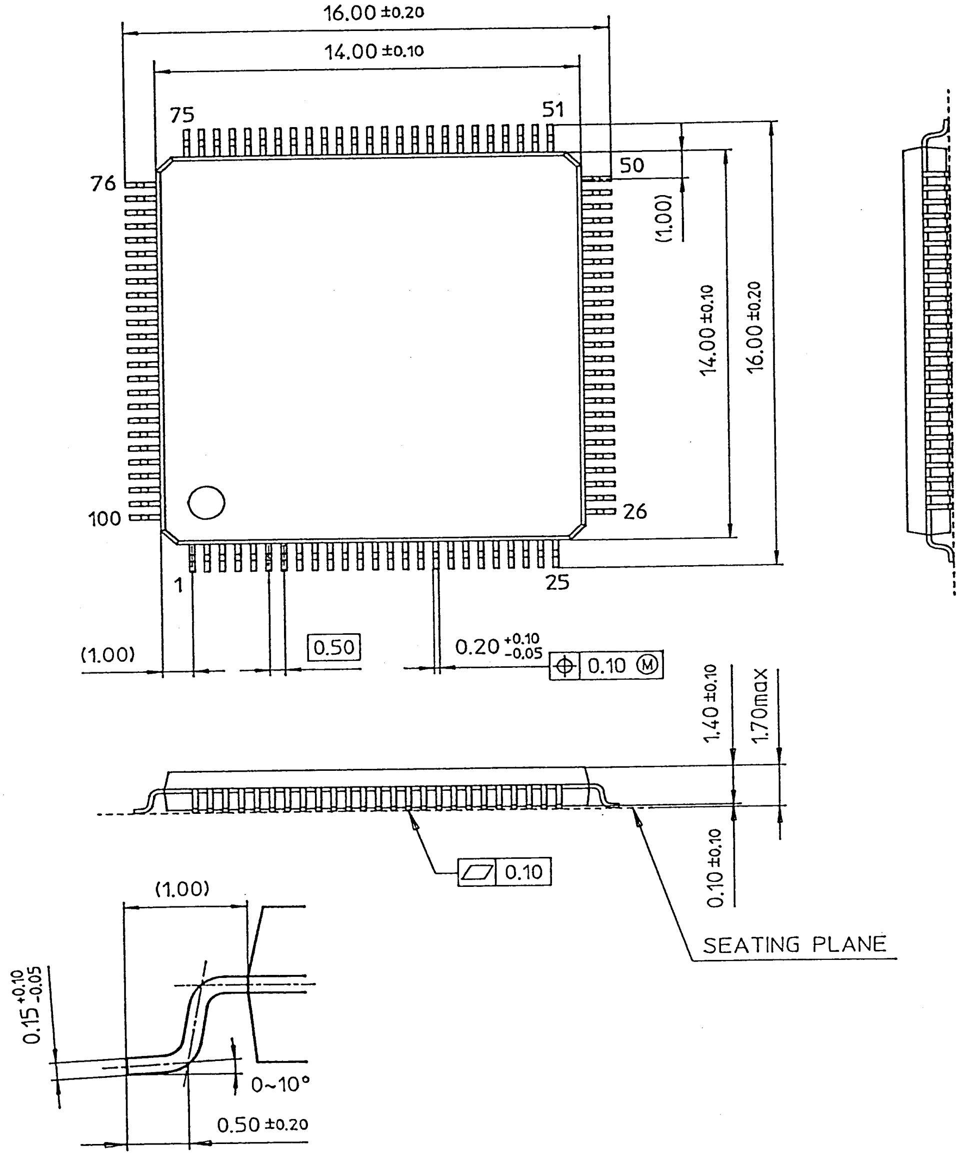


Figure 1-4-3 Reset Connection Example

1-5 Package Dimension

Package Code: LQFP064-P-1414   unit: mm



Body Material: Epoxy Resin, Lead Material: Cu Alloy, Lead Finish Method: Pd Plating

Figure 1-5-1   64-pin LQFP

The package dimension is subject to change. Before using this product, please obtain product specifications from the sales office.

Chapter 2 Memory Configuration

2-1 Memory Configuration

2-1-1 Overview

This series operates at the single chip mode.

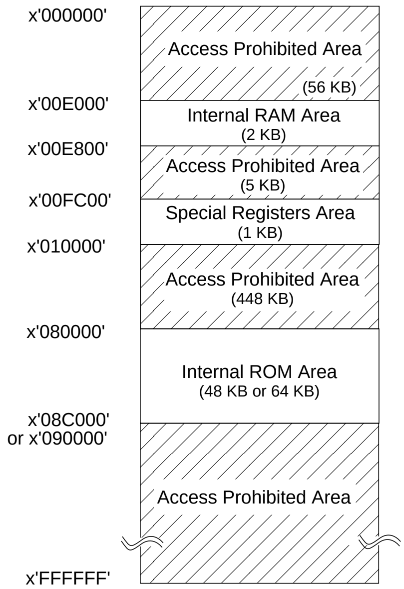


Figure 2-1-1 Address Space

2-1-2 Control Registers

Memory is controlled by the memory control register (MEMCTR) and the system control register (SYSCTL).

Table 2-1-1 Control Registers

Register Symbol	Address	R/W	Register Name
MEMCTR	X'00FC02'	R/W	Memory control register
SYSCTL	X'00FC32'	R/W	System control register

MEMCTR has to be set up to be agreeable to the system configuration in the initialization program.

MEMCTR register of this series sets up x'04n0' (n=0 to 3: These are wait number of the special register. 1 is usual.) in the initialization program.

Chapter 3 Interrupts

3-1 Interrupt Groups

3-1-1 Overview

The interrupt controller contains eight groups. Each group has some interrupt vectors . When an interrupt occurs, the CPU receives an interrupt request. [☞ MN10200 Series LSI User’s Manual Linear Addressing Version]

Table 3-1-1 List of Interrupt Control Registers

Interrupt Group	Interrupt Vector (Number is IDTn bit position)	Control Register
Group 0	2 Undefined Instruction Interrupt 1 Watchdog Timer Interrupt 0 NMI Interrupt	Non-maskable Interrupt Control Register 0 G0ICR: x'00FC40'
Group 1	3 Timer/Counter 0 Underflow 2 External Interrupt IRQ2 1 External Interrupt IRQ1 0 External Interrupt IRQ0	Maskable Interrupt Control Register 1 G1ICR: x'00FC42'
Group 2	3 A/D Conversion End 2 External Interrupt IRQ5 1 External Interrupt IRQ4 0 External Interrupt IRQ3	Maskable Interrupt Control Register 2 G2ICR: x'00FC44'
Group 3	3 Reserved 2 Serial Ch0 Transmission End 1 Timer/Counter 2 Underflow 0 Timer/Counter 1 Underflow	Maskable Interrupt Control Register 3 G3ICR: x'00FC46'
Group 4	3 Reserved 2 Serial Ch1 Transmission End 1 Timer/Counter 8 Underflow 0 Timer/Counter 3 Underflow	Maskable Interrupt Control Register 4 G4ICR: x'00FC48'
Group 5	3 Reserved 2 Timer/Counter 9 Underflow 1 Timer/Counter 5 Underflow 0 Timer/Counter 4 Underflow	Maskable Interrupt Control Register 5 G5ICR: x'00FC4A'
Group 6	3 Reserved 2 Reserved 1 Timer/Counter 6 Underflow 0 Timer/Counter 10 Overflow	Maskable Interrupt Control Register 6 G6ICR: x'00FC4C'
Group 7	3 Unavailable (Set the corresponding enable flag always to 0.) 2 Unavailable (Set the corresponding enable flag always to 0.) 1 Timer/Counter 7 Underflow 0 Timer/Counter 11 Underflow/Overflow	Maskable Interrupt Control Register 7 G7ICR: x'00FC4E'

Reserved: A corresponding flag does not actually exist.

Change of G1ICR interrupt level (ILVn) and interrupt enable flag (IENn) should be executed when PSW enable flag (IE) is 0.

The control registers are assigned to each corresponding interrupt group except Group 0 and control the assigned interrupt vectors. For example, in the MN102L(F) 59x, when timer 0 becomes underflow, the interrupt request flag (IRF3=TM0IR) of the maskable interrupt control register 1 (G1ICR) becomes 1. At this point, an interrupt request is output to the CPU core if the corresponding interrupt enable flag (IEN3=TM0IE) is 1. Comparing the interrupt mask level (IM2 to 0) of the processor status word (PSW) with the group interrupt level (ILVn=G1LV[2:0]) of the G1ICR register and the interrupt enable flag (IE) of PSW determine whether the CPU core receives the interrupt or not.

G1ICR: x'00FC42'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	G1 LV2	G1 LV1	G1 LV0	TM0 IE	IRQ2 IE	IRQ1 IE	IRQ0 IE	TM0 IR	IRQ2 IR	IRQ1 IR	IRQ0 IR	TM0 ID	IRQ2 ID	IRQ1 ID	IRQ0 ID

Group interrupt level
ILVn
Setup of interrupt level

Interrupt enable flag
IENn
Setup of interrupt permission

Interrupt demand flag
IRFn
Occurrence of interrupt factor

Interrupt detective flag
IDTn
Detection of interrupt demand

Please refer to "2-5 Interrupt Controller" in the MN10200 Series LSI User's Manual Linear Addressing Version for detail operations, and the MN10200 Series Instruction Manual Linear Addressing Version for interrupt handling flow and handler programming.

> Set the interrupt enable flags IEN [3:2] (bits [11:10]) of the G7ICR always to 0.

3-2 External Interrupts

3-2-1 External Pin Interrupts

Group 1 to Group 5 control external pin interrupts.

The EXTMD register sets the interrupt conditions.

The EXTMD register sets the interrupt levels and timing of external interrupts, and specifies each pins' level or edge.

EXTMD: x'00FC50'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	IRQ5 TG1	IRQ5 TG0	IRQ4 TG1	IRQ4 TG0	IRQ3 TG1	IRQ3 TG0	IRQ2 TG1	IRQ2 TG0	IRQ1 TG1	IRQ1 TG0	IRQ0 TG1	IRQ0 TG0

EIRQ5 EIRQ4 EIRQ3 EIRQ2 EIRQ1 EIRQ0

00: An interrupt occurs at low level.
01: An interrupt occurs at high level.
10: An interrupt occurs at negative edge.
11: An interrupt occurs at positive edge.

3-2-2 NMI Pin Interrupts

This series supports an NMI interrupt. The $\overline{\text{NMI}}$ interrupt occurs on the negative edge of NMI pin.

3-2-3 External Pin Interrupt Noise Filter

External interrupt pins IRQ0 to IRQ3 and NMI have the built-in noise clearing circuit.

NFCTR: x'00FC52'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	IRQ3 FSE	IRQ3 FEN	IRQ2 FSE	IRQ2 FEN	IRQ1 FSE	IRQ1 FEN	IRQ0 FSE	IRQ0 FEN	NMI SEL1	NMI SEL0

IRQ3 IRQ2 IRQ1 IRQ0 NMI

IRQnFEN 0: Noise filter is off.
1: Noise filter is on.

IRQnFSE 0: Sampling at 2^2 machine cycle
1: Sampling at 2^7 machine cycle

NMI:
00: Sampling at 1 machine cycle
01: Sampling at 2^2 machine cycle
10: Sampling at 2^7 machine cycle
11: unavailable

The waveform that is input from the interrupt pins is sampled. As for IRQ0 to IRQ3, when low level interrupt or negative edge interrupt is set, if low level is input for more than 4 sampling periods, an interrupt signal is input inside of CPU. When high level interrupt or positive edge interrupt is set, if high level is input for more than 4 sampling periods, an interrupt signal is input inside of CPU.

> The noise filter is unavailable at STOP mode and HALT mode.

3-3 Interrupt Setup Examples

3-3-1 External Pin Interrupt Setup

An interrupt occurs on the negative (falling) edge from the external interrupt pin IRQ0 (P20).

The external interrupt edge specification register (EXTMD) is set to the interrupt request generation at low level after reset release, and the IRQ0IR bit of the maskable interrupt control register 1 (G1ICR) becomes 0.

■ Interrupt Enable Setup

(1) Set the interrupt conditions of the interrupt pin IRQ0 (P20). In this case, set the IRQ0TG of the EXTMD register to 2 (bit string 10:negative edge).

EXTMD: x'00FC50'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	IRQ5 TG1	IRQ5 TG0	IRQ4 TG1	IRQ4 TG0	IRQ3 TG1	IRQ3 TG0	IRQ2 TG1	IRQ2 TG0	IRQ1 TG1	IRQ1 TG0	IRQ0 TG1	IRQ0 TG0
-	-	-	-	0	0	0	0	0	0	0	0	0	0	1	0

In this example, the interrupt level is 4.

(2) Enable interrupts. At this point, clear all prior interrupt requests. To do this, set G1LV[2:0], IRQ0IR and IRQ0IE of the maskable interrupt control register 1 (G1ICR) to an interrupt level, 0 and 1, respectively.

G1ICR: x'00FC42'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	G1 LV2	G1 LV1	G1 LV0	TM0 IE	IRQ2 IE	IRQ1 IE	IRQ0 IE	TM0 IR	IRQ2 IR	IRQ1 IR	IRQ0 IR	TM0 ID	IRQ2 ID	IRQ1 ID	IRQ0 ID
-	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

(3) Enable interrupts by setting the interrupt enable flag (IE) of the processor status Word (PSW) to 1 and the interrupt mask level (IMn) to 7 (bit string 111).

Thereafter, an interrupt occurs when the negative (falling) edge is generated on the interrupt pin IRQ0 (P20). The program branches to x'080008' when the interrupt is accepted.

■ Interrupt Handling

(4) Specify the interrupt group by reading the interrupt accept group register (IAGR) during interrupt prehandling.

Normally, the program generates the interrupt start address and branches to that address.

(5) Specify the interrupt vector in the group by reading the G1ICR register. Check the IRQ0ID with the bit test instruction (BTST). If IRQ0ID is 1, execute the interrupt handling.

During interrupt service routine, the IM and IE of PSW become the interrupt level and 0 respectively. The multiple interrupts are not allowed. It means that other interrupts except the non-maskable interrupt are not accepted during interrupt service routine unless the PSW is set.

(6) Clear the IRQ0IR bit of the G1ICR register.

(7) Return to the main program with the interrupt return instruction (RTI) after the interrupt handling ends.

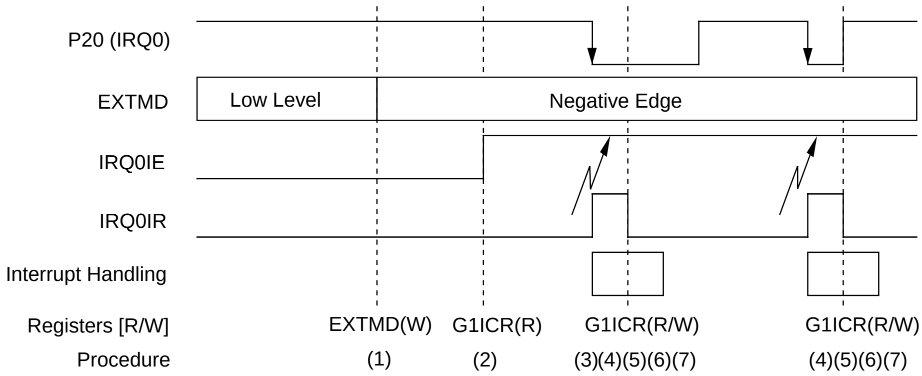


Figure 3-3-1 External Pin Interrupt Timing

3-3-2 Watchdog Timer Interrupt

An interrupt occurs by using the watchdog timer.

When the watchdog fanction is used, operation is started by setting the WDRST flag of the CPU mode control register (CPUM) to enable ('0') after reset. The watchdog timer needs to be cleared during the main program because a non-maskable interrupt occurs when the watchdog counter overflows.

When the watchdog timer counts 65536 cycles of SYSCLK (6.5536 ms with a 20-MHz oscillator), a watchdog interrupt occurs. Watch-dog interrupt occurring term can be extended 8, 16 or 32 times by the watchdog timer expansion control register.

■ Interrupt Enable Setup

(1) Enable interrupts by setting the interrupt enable flag (IE) of the processor status Word (PSW) to 1 and the interrupt mask level (IMn) to 7 (bit string 111).

(2) Clear the WDRST flag of the CPUM register. This starts the watchdog timer.

CPUM: x'00FC00'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD RST	WD LNG1	WD LNG0	—	—	—	—	—	—	—	—	OSC ID	STOP	HALT	OSC1	OSC2
0	0	0	-	-	-	-	-	-	-	-	0	0	0	0	0

Normally, clear the watchdog timer before an interrupt occurs.

■ Watchdog Timer Clear

(3) Set the WDRST flag of the CPUM register to 1 and then immediately clear to 0. The watchdog timer is cleared to 0 when the WDRST flag is 1.

Normally, the program generates the interrupt start address and branches to that address.

■ Interrupt Handling

The program branches to x'080008' when an interrupt is generated and accepted.

(4) Specify the interrupt group by reading the interrupt accept group register (IAGR) during interrupt prehandling.

The IM of PSW becomes the highest level during interrupt handling and other interrupts are not accepted.

(5) Verify a watchdog interrupt by reading the nonmaskable interrupt control register (G0ICR). Check the WDIF with the bit test instruction (BTST). If WDIF is 1, execute the interrupt service routine.

(6) Clear the WDIF flag of the G0ICR register.

(7) Return to the main program with the interrupt return instruction (RTI) after the interrupt handling ends.

The watchdog timer and the oscillation stabilization wait counter are shared. The watchdog timer operates as the oscillation stabilization wait counter when the CPU returns from the STOP mode. Because of this, the WDIF flag is cleared to 0 when the CPU moves to the STOP mode. The WDIF flag is cleared to 0 again after the CPU moves to the normal mode. [☞ "2-6 Standby Function" in the MN10200 Series LSI User's Manual Linear Addressing Version]

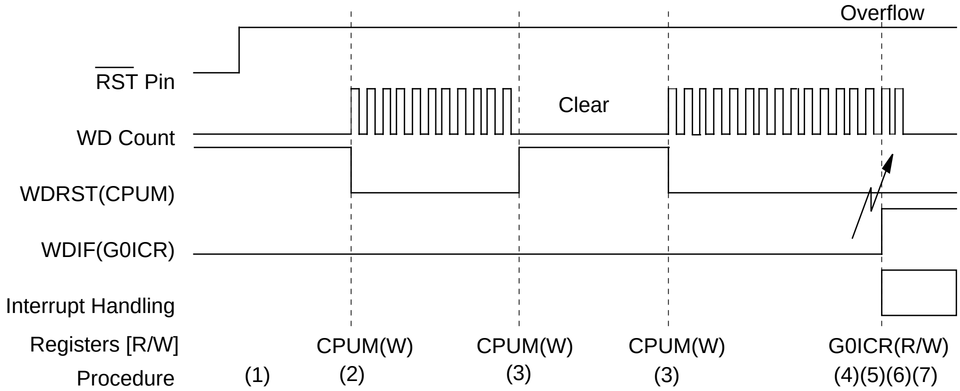


Figure 3-3-2 Watchdog Timer Interrupt Timing

Chapter 4 Timers

4-1 Timers

4-1-1 Overview

This LSI series contains nine 8-bit timers (timer 0 to timer 5 and timer 8 to timer 10) and three 16-bit timers (timer 6, timer 7 and timer11).

Table 4-1-1 Timer Function (1/3)

Function \ Timer	8-bit Timer			
	Timer 0	Timer 1	Timer 2	Timer 3
Interrupt Request Destination	Group 1 (G1ICR) - TM0IR	Group 3 (G2ICR) - TM1IR	Group 3 (G3ICR) - TM2IR	Group 4 (G4ICR) - TM3IR
Interrupt Source	Timer 0 underflow	Timer 1 underflow	Timer 2 underflow	Timer 3 underflow
Clock Source	- TM0IO pin - ϕ/128 *1 - ϕ *2 - ϕ/64 *3	- TM1IO pin - ϕ/64 - Timer 0 - ϕ	- TM2IO pin - Timer 1 - Timer 0 - ϕ	- ϕ/64 - ϕ/2 *4 - Timer 0 - ϕ
Counting Method	Down counting	Down counting	Down counting	Down counting
Interval Timer	√	√	√	√
Event Counter	√	√	√	-
Timer Output	√	√	√	-
PWM	-	-	-	-
One-phase Capture Input	-	-	-	-
External Count Direction Control	-	-	-	-
Serial Interface Transfer Clock Generation	-	-	-	√
A/D Conversion Timing Generation	-	√	-	-

*1 System Clock (10 MHz with 5-MHz external oscillation)/128
*2 System Clock (10 MHz with 5-MHz external oscillation)
*3 System Clock (10 MHz with 5-MHz external oscillation)/64
*4 System Clock (10 MHz with 5-MHz external oscillation)/2

Table 4-1-1 Timer Function (2/3)

Function \ Timer	8-bit Timer		16-bit Timer	
	Timer 4	Timer 5	Timer 6	Timer 7
Interrupt Request Destination	Group 5 (G5ICR) - TM4IR	Group 5 (G1ICR) - TM5IR	Group 6 (G6ICR) - TM6IR	Group 7 (G7ICR) - TM7IR
Interrupt Source	Timer 4 underflow	Timer 5 underflow	Timer 6 underflow	Timer 7 underflow
Clock Source	- ϕ/128 - ϕ/64 - Timer 0 - ϕ	- ϕ/64 - Timer 4 - Timer 0 - ϕ	- ϕ - Timer 0 - ϕ/128 - TM6IO pin	- ϕ - Timer 0 - ϕ/128 - TM7IO pin
Counting Method	Down counting	Down counting	Up/down counting	Up/down counting
Interval Timer	√	√	√	√
Event Counter	-	-	√	√
Timer Output	-	-	√	√
PWM	-	-	Optional duty	Optional duty
One-phase Capture Input	-	-	√	√
External Count Direction Control	-	-	√	√
Serial Interface Transfer Clock Generation	-	-	-	-
A/D Conversion Timing Generation	-	-	-	-

Table 4-1-1 Timer Function (3/3)

Function \ Timer	8-bit Timer			16-bit Tlimer
	Timer 8	Timer 9	Timer 10	Timer 11
Interrupt Request Destination	Group 4 (G4ICR) - TM8IR	Group 5 (G5ICR) - TM9IR	Group 6 (G6ICR) - TM10IR	Group 7 (G7ICR) - TM11IR
Interrupt Source	Timer 8 underflow	Timer 9 underflow	Timer 10 overflow (According with Timer 10 compare A)	Timer 11 underflow/overflow
Clock Source	- Timer 0 - φ/8 - TM8IO pin - φ/2	- Timer 0 - φ/8 - TM9IO pin - φ/2	- Internal OSC clock - φ/8 - φ - φ/2	- Internal OSC clock - φ
Counting Method	Up/down counting	Up/down counting	Up/down counting	Up/down counting
Interval Timer	√	√	√	√
Event Counter	√	√	-	-
Timer Output	√	√	√	√
PWM	Optional duty	Optional duty	Simplified 6-phase output	6-phase output
One-phase Capture Input	√	√	-	-
External Count Direction Control	√	√	-	-
Serial Interface Transfer Clock Generation	-	-	-	-
A/D Conversion Timing Generation	-	-	-	√

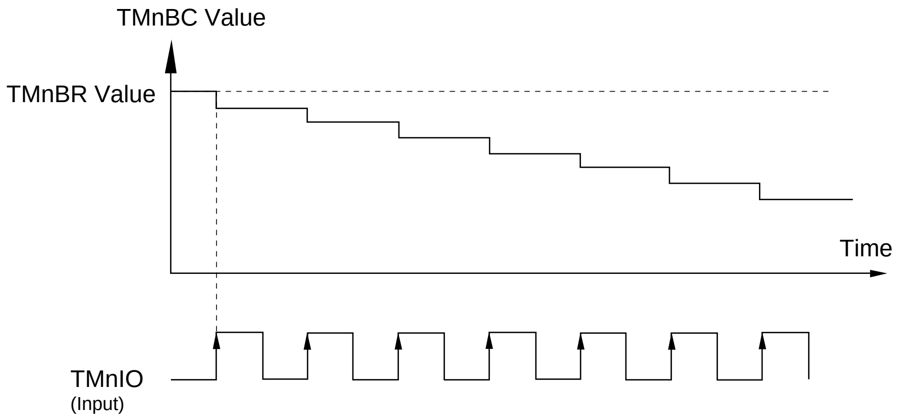


Figure 4-1-1 Event Counter Timing (Timer 0 to Timer 2)

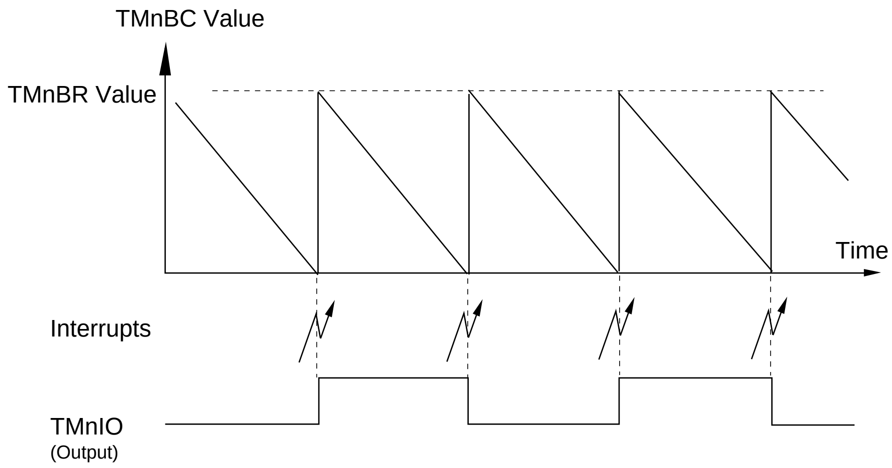


Figure 4-1-2 Timer Output, Interval Timer* Timing (Timer 0 to Timer 5)
*Timer 3 to Timer 5 only have interval timer function.

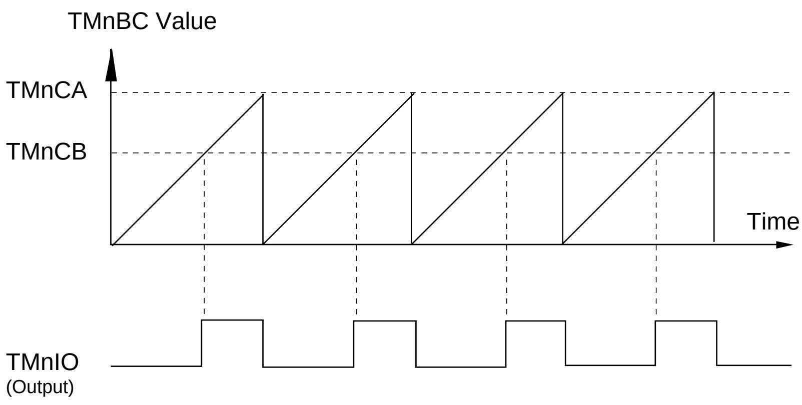


Figure 4-1-3 PWM Output Timing (Timer 6 to Timer 9)

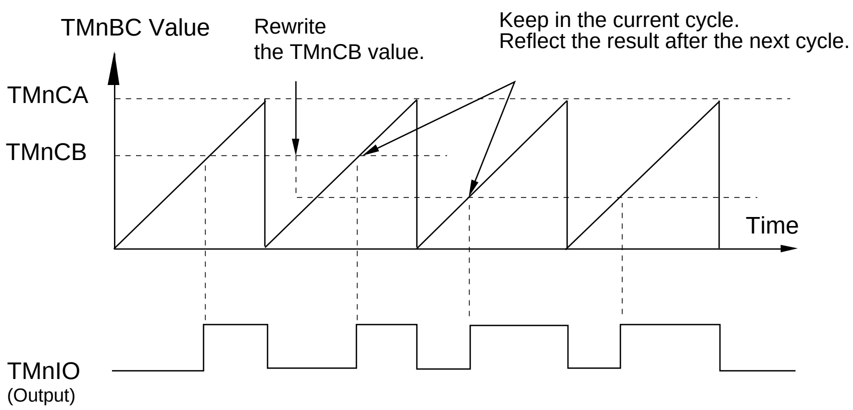


Figure 4-1-4 PWM Output Timing (Compensated at Data Write) (Timer 6 to Timer 9)

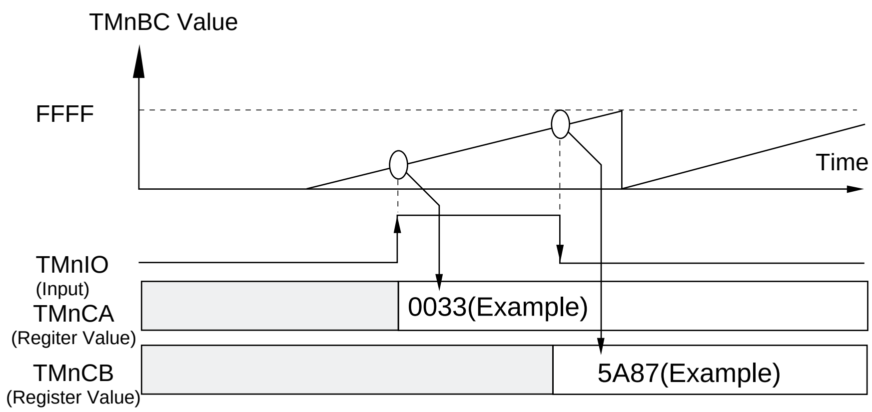


Figure 4-1-5 One-phase Capture Input Timing (Timer 6 to Timer 9)

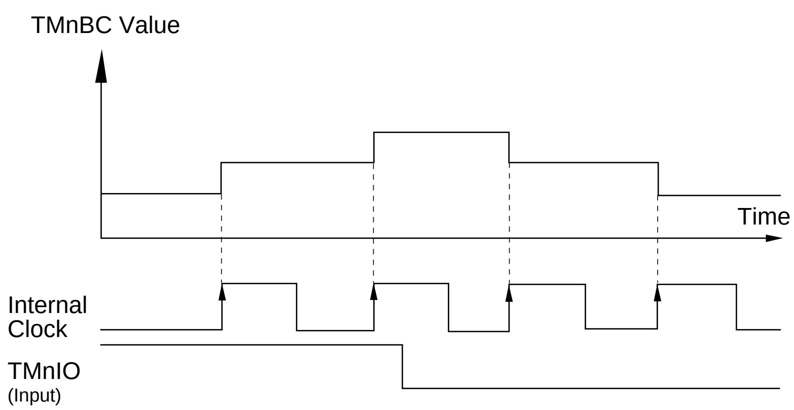


Figure 4-1-6 External Count Direction Control Timing (Timer 6 to Timer 9)

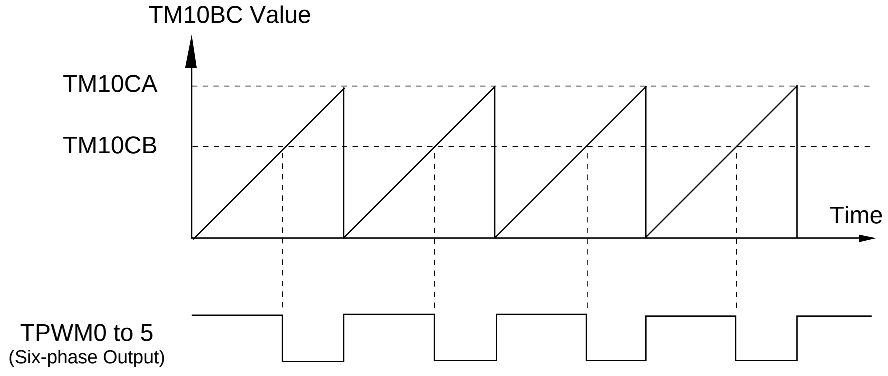


Figure 4-1-7 PWM Output Timing (Timer10)

■ Timer 0 to Timer 5

Timer 0 to Timer 5 are 8-bit timers. They are down counting and are divided by the 8-bit value, that is set in the base register (TMnBR), plus one. (Do not set 0 to TMnBR). An interrupt occurs when each timer underflows (the binary counter value changes from x'00' to the 8-bit value). They can be used for interval timers, event counters, clock output, base clock for serial interface and A/D conversion start timing.

Timer 1, timer 2, timer 4 and timer 5 can be connected in cascade arrangement. Cascading timer 1 and timer 2 can form as a 16-bit timer. Cascading timer 4 and timer 5 can form as a 16-bit timer. That means these timers can form a 16-bit timer at most.

■ Timer 6 and Timer 7

Timer 6 and Timer 7 are 16-bit timers. They are up/down counting. Each timer has two compare/capture registers (TMnCA and TMnCB) to capture the up/down counter value, compare the binary counter value with the compare capture register value and generate PWM and interrupts. The timers contain the double buffer mode that changes the cycle and transition after the next cycle at PWM generation. This prevents the PWM waveform losses and distorts during timing changes. They can be used for interval timers, event counters (at clock oscillation), one-phase PWM, one-phase capture and external count direction controllers.

An underflow interrupt occurs only when these timers are down counting.

■ Timer 8 and Timer 9

Timer 8 and Timer 9 are 8-bit timers. They are up/down counting. Each timer has two compare/capture registers (TMnCA and TMnCB) to capture the up/down counter value, compare the binary counter value with the compare capture register value and generate PWM and interrupts. The timers contains the double buffer mode that changes the cycle and transition after the next cycle at PWM generation. This prevents the PWM waveform losses and distorts during timing changes. They can be used for interval timers, event counters (at clock oscillation), one-phase PWM, one-phase capture and external count direction controllers.

■ Timer 10

Timer 10 is a 8-bit timer. This is up/down counting. It has two compare registers (TM10CA and TM10CB) to compare the binary counter value with the compare capture register value and generates six-phase PWM and interrupts. It contains the double buffer mode that changes the cycle and transition after the next cycle at the six-phase PWM generation. This prevents the PWM waveform losses and distorts during timing changes. When the six-phase PWM is output, fixed output to each pin is possible by port control.

■ Timer 11

Timer 11 is a 16-bit timer for inverter motor control. The three-phase (U-phase, V-phase and W-phase) PWM output is possible. PWM cycle is set by 16-bit counter that is synchronized with a microcontroller clock. PWM pulse width can be set by the three-phase independent compare register. This contains the double buffer mode that prevents the PWM waveform losses and distorts during timing changes. Dead time can be set.

The timer configuration is shown below. Combination of several timers offers various kinds of interval timers. They are explained in Timer Setup Examples.

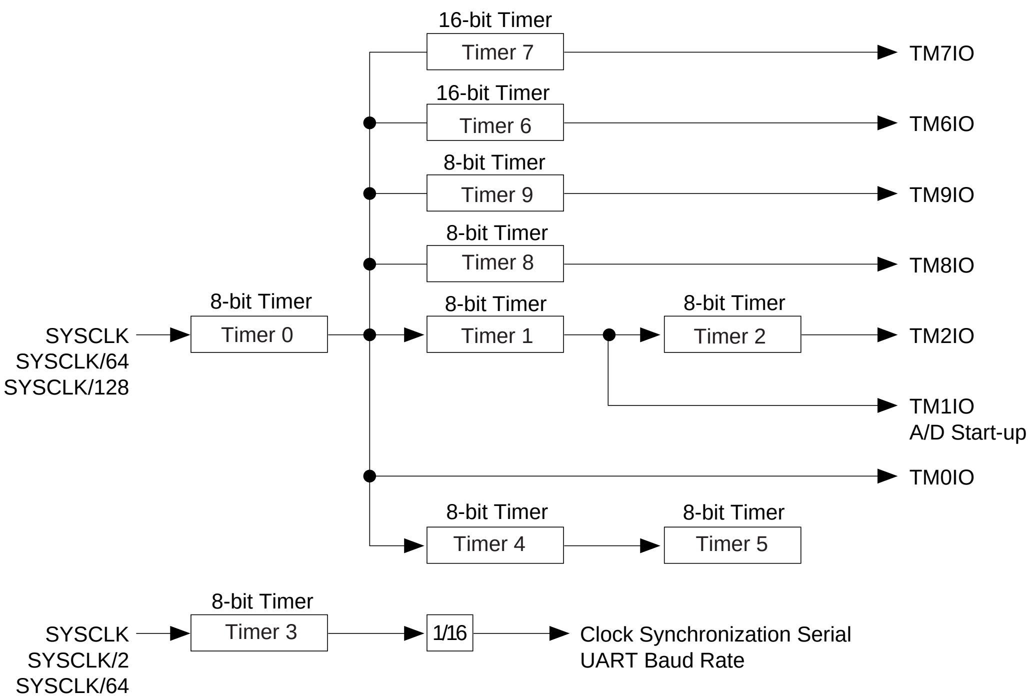


Figure 4-1-8 System Configuration

4-1-2 Timer Control Registers

The following tables show timer control registers.

Table 4-1-2 Timer Control Registers (1/2)

Register Symbol		Address	R/W	Register Name
Timer 0	TM0MD	x'00FE20'	R/W	Timer 0 Mode Register
	TM0BC	x'00FE00'	R	Timer 0 Binary Counter
	TM0BR	x'00FE10'	R/W	Timer 0 Base Register
Timer 1	TM1MD	x'00FE21'	R/W	Timer 1 Mode Register
	TM1BC	x'00FE01'	R	Timer 1 Binary Counter
	TM1BR	x'00FE11'	R/W	Timer 1 Base Register
Timer 2	TM2MD	x'00FE22'	R/W	Timer 2 Mode Register
	TM2BC	x'00FE02'	R	Timer 2 Binary Counter
	TM2BR	x'00FE12'	R/W	Timer 2 Base Register
Timer 3	TM3MD	x'00FE23'	R/W	Timer 3 Mode Register
	TM3BC	x'00FE03'	R	Timer 3 Binary Couter
	TM3BR	x'00FE13'	R/W	Timer 3 Base Register
Timer 4	TM4MD	x'00FE24'	R/W	Timer 4 Mode Register
	TM4BC	x'00FE04'	R	Timer 4 Binary Counter
	TM4BR	x'00FE14'	R/W	Timer 4 Base Register
Timer 5	TM5MD	x'00FE25'	R/W	Timer 5 Mode Register
	TM5BC	x'00FE05'	R	Timer 5 Binary Counter
	TM5BR	x'00FE15'	R/W	Timer 5 Base Register
Timer 6	TM6MD	x'00FE30'	R/W	Timer 6 Mode Register
	TM6BC	x'00FE32'	R	Timer 6 Binary Counter
	TM6CA	x'00FE34'	R/W	Timer 6 Compare/Capture Register A
	TM6CAX	x'00FE36'	-	Timer 6 Compare/Capture Register Set A
	TM6CB	x'00FE38'	R/W	Timer 6 Compare/Capture Register B
	TMCBX	x'00FE3A'	-	Timer 6 Compare/Capture Register Set B
Timer 7	TM7MD	x'00FE40'	R/W	Timer 7 Mode Register
	TM7BC	x'00FE42'	R	Timer 7 Binary Counter
	TM7CA	x'00FE44'	R/W	Timer 7 Compare/Capture Register A
	TM7CAX	x'00FE46'	-	Timer 7 Compare/Capture Register Set A
	TM7CB	x'00FE48'	R/W	Timer 7 Compare/Capture Register B
	TM7CBX	x'00FE4A'	-	Timer 7 Compare/Capture Register Set B

TM6CAX, TM6CBX, TM7CAX and TM7CBX are dummy registers used for specifying double buffer mode at PWM output. They do not exist.

Table 4-1-2 Timer Control Registers (2/2)

Register Symbol		Address	R/W	Register Name
Timer 8	TM8MD	x'00FE50'	R/W	Timer 8 Mode Register
	TM8BC	x'00FE52'	R	Timer 8 Binary Counter
	TM8CA	x'00FE54'	R/W	Timer 8 Compare/Capture Register A
	TM8CAX	x'00FE56'	-	Timer 8 Compare/Capture Register Set A
	TM8CB	x'00FE58'	R/W	Timer 8 Compare/Capture Register B
	TM8CBX	x'00FE5A'	-	Timer 8 Compare/Capture Register Set B
Timer 9	TM9MD	x'00FE60'	R/W	Timer 9 Mode Register
	TM9BC	x'00FE62'	R	Timer 9 Binary Counter
	TM9CA	x'00FE64'	R/W	Timer 9 Compare/Capture Register A
	TM9CAX	x'00FE66'	-	Timer 9 Compare/Capture Register Set A
	TM9CB	x'00FE68'	R/W	Timer 9 Compare/Capture Register B
	TM9CBX	x'00FE6A'	-	Timer 9 Compare/Capture Register Set B
Timer 10	TM10MD	x'00FE70'	R/W	Timer 10 Mode Register
	TM10BC	x'00FE72'	R	Timer 10 Binary Counter
	TM10CA	x'00FE74'	R/W	Timer 10 Compare/Capture Register A
	TM10CAX	x'00FE76'	-	Timer 10 Compare/Capture Regsiter Set A
	TM10CB	x'00FE78'	R/W	Timer 10 Compare/Capture Register B
	TM10CBX	x'00FE7A'	-	Timer 10Compare/Capture Register Set B
Timer 11	TM11MD	x'00FE80'	R/W	Timer 11 Mode Control Register
	TM11EX	x'00FE82'	R/W	Timer 11 Output Polar Control Register
	TM11SL	x'00FE84'	R/W	Timer 11 Output Control Register
	TM11BR	x'00FE86'	R/W	Timer 11 Cycle Setting Register
	TM11CA	x'00FE88'	R/W	Timer 11 U-phase Compare Setting Register
	TM11CB	x'00FE8A'	R/W	Timer 11 V-phase Compare Setting Register
	TM11CC	x'00FE8C'	R/W	Timer 11 W-phase Compare Setting Register
	TM11DT	x'00FE8E'	R/W	Timer 11 Dead Time Setting Register
	TM11CK	x'00FE90'	R/W	Timer 11 Clock Source Selection Register
Buzzer Output	WDREG	x'00FC54'	R/W	Watchdog Expansion and Buzzer Output Control Register

TM8CAX, TM8CBX, TM9CAX, TM9CBX, TM10CAX and TM10CBX are dummy registers used for specifying double buffer mode at PWM output. They do not exist.

4-1-3 Timer Block Diagrams

This section describes block diagrams of timer 0 to timer 11.

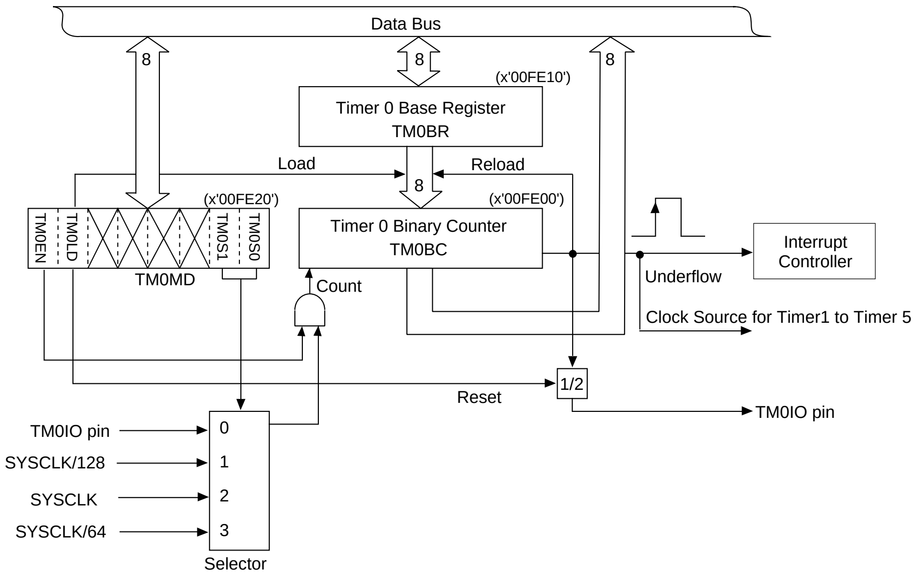


Figure 4-1-9 Timer 0 Block Diagram

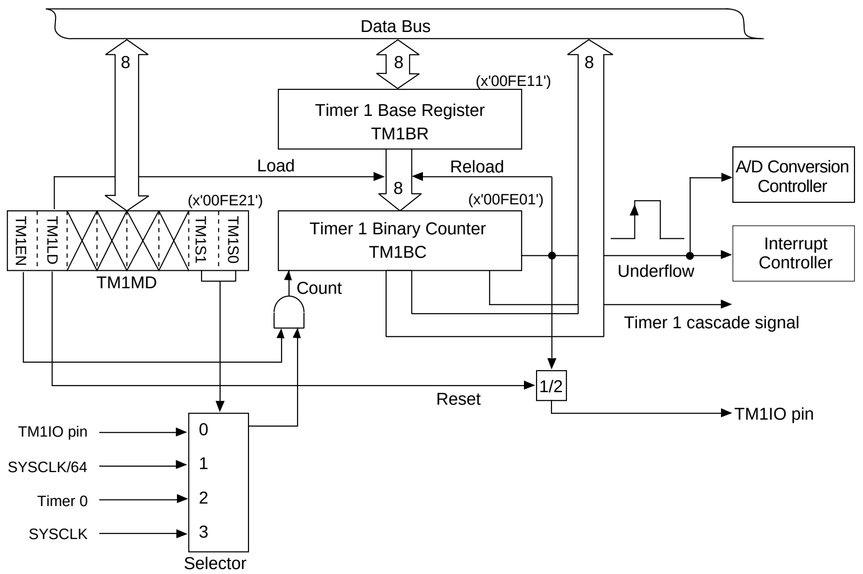


Figure 4-1-10 Timer 1 Block Diagram

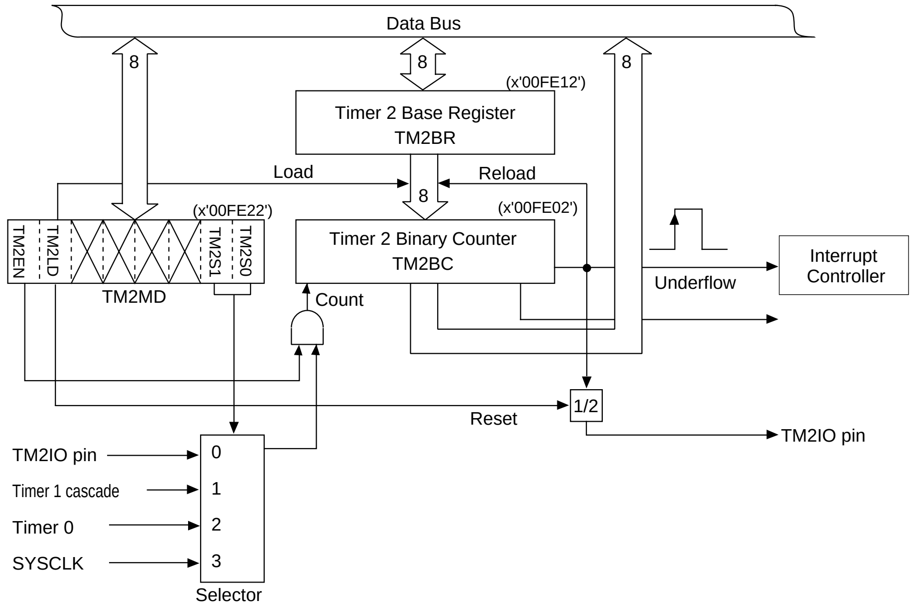


Figure 4-1-11 Timer 2 Block Diagram

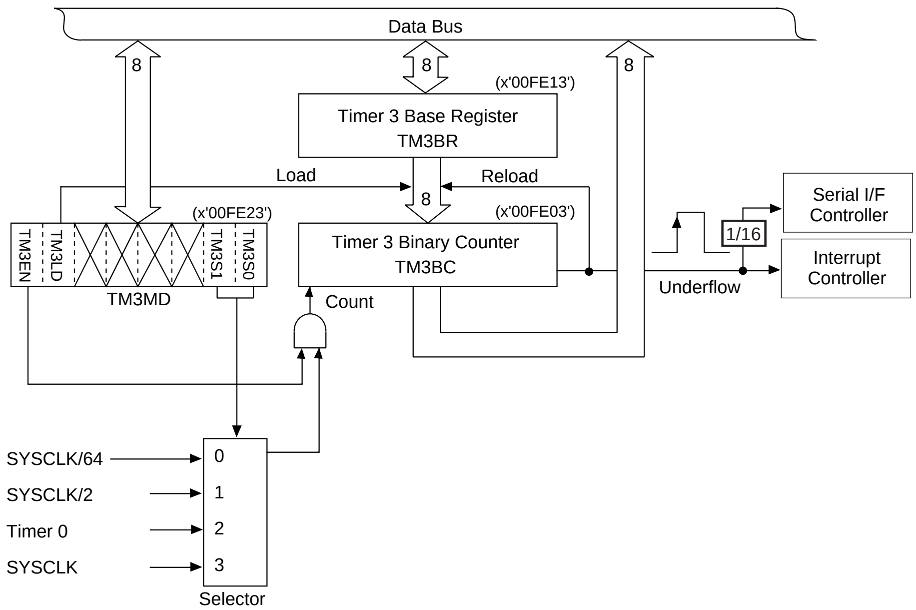


Figure 4-1-12 Timer 3 Block Diagram

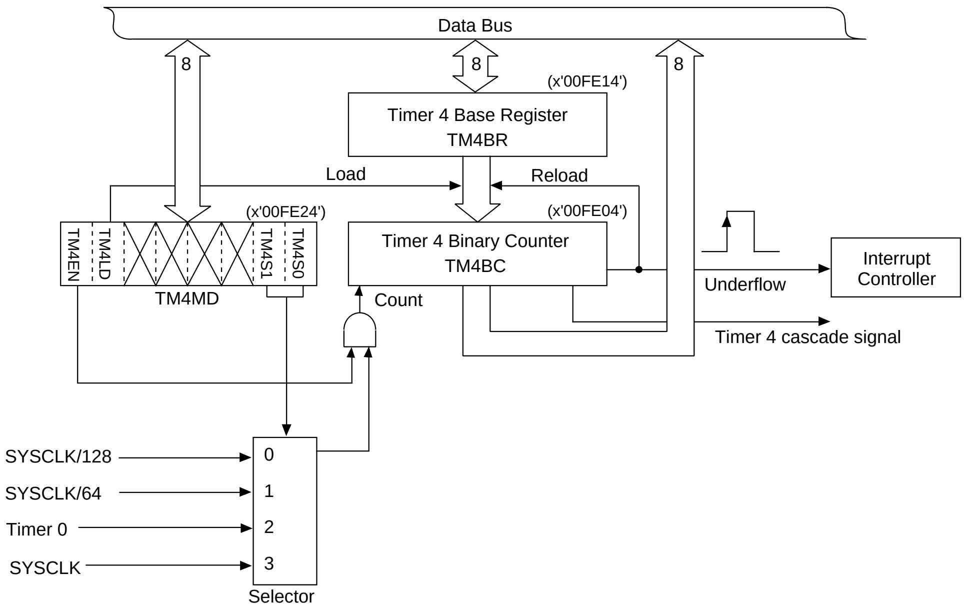


Figure 4-1-13 Timer 4 Block Diagram

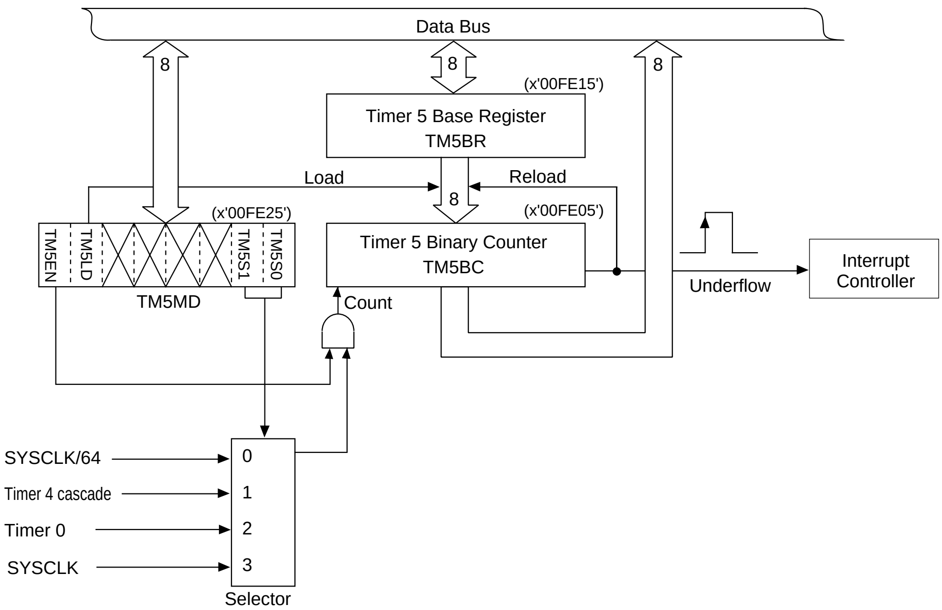


Figure 4-1-14 Timer 5 Block Diagram

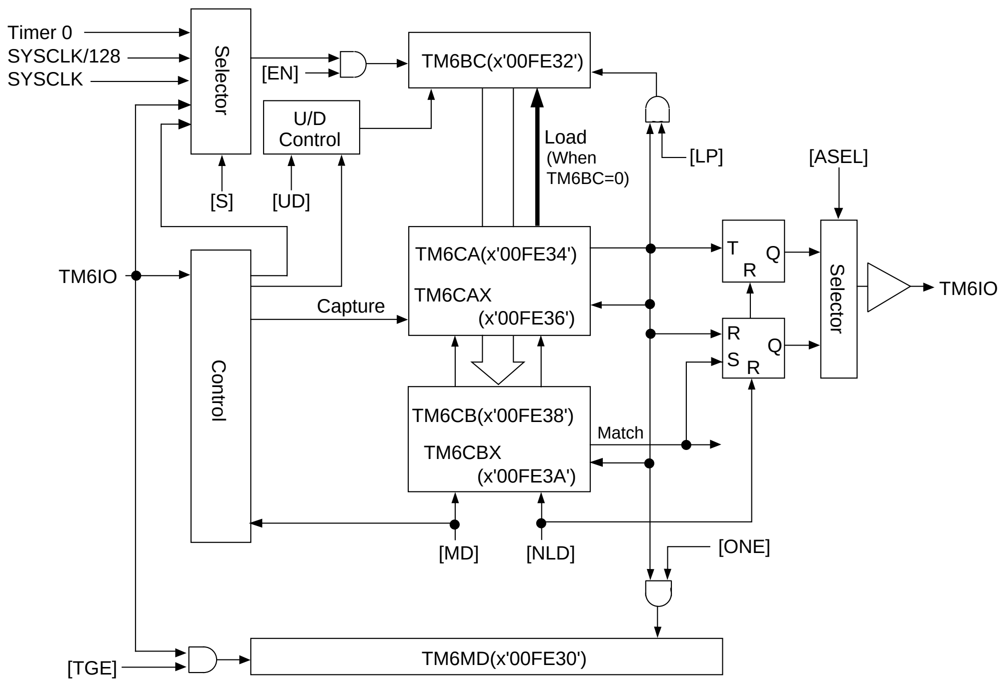


Figure 4-1-15 Timer 6 Block Diagram

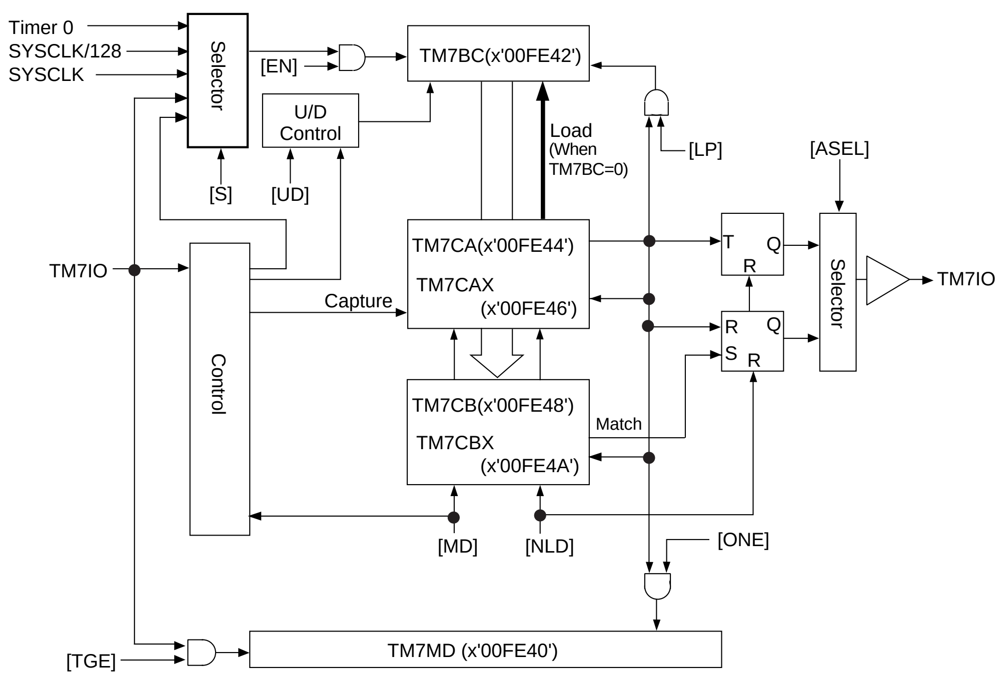


Figure 4-1-16 Timer 7 Block Diagram

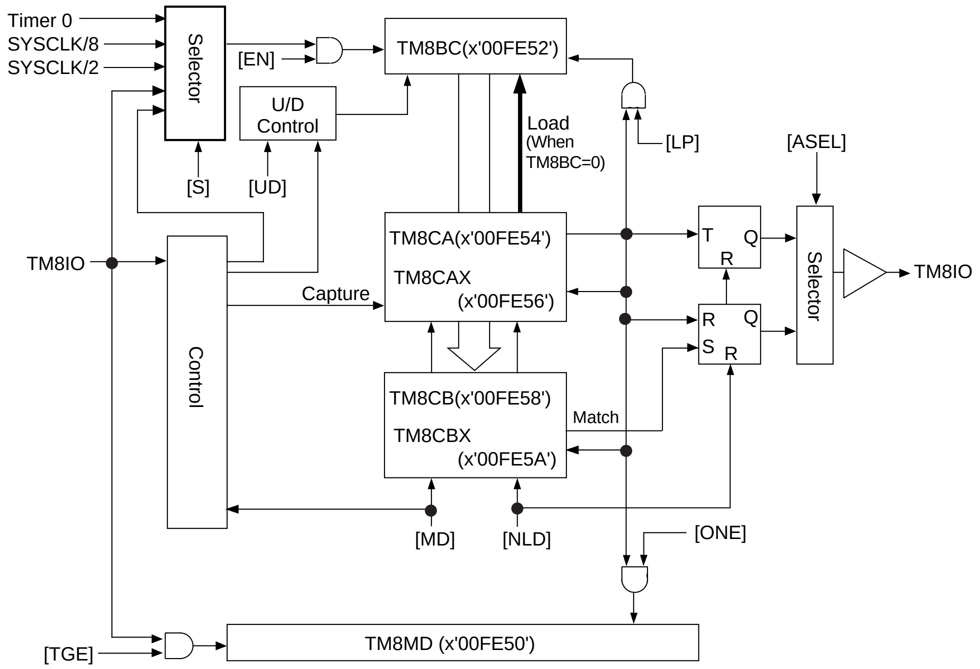


Figure 4-1-17 Timer 8 Block Diagram

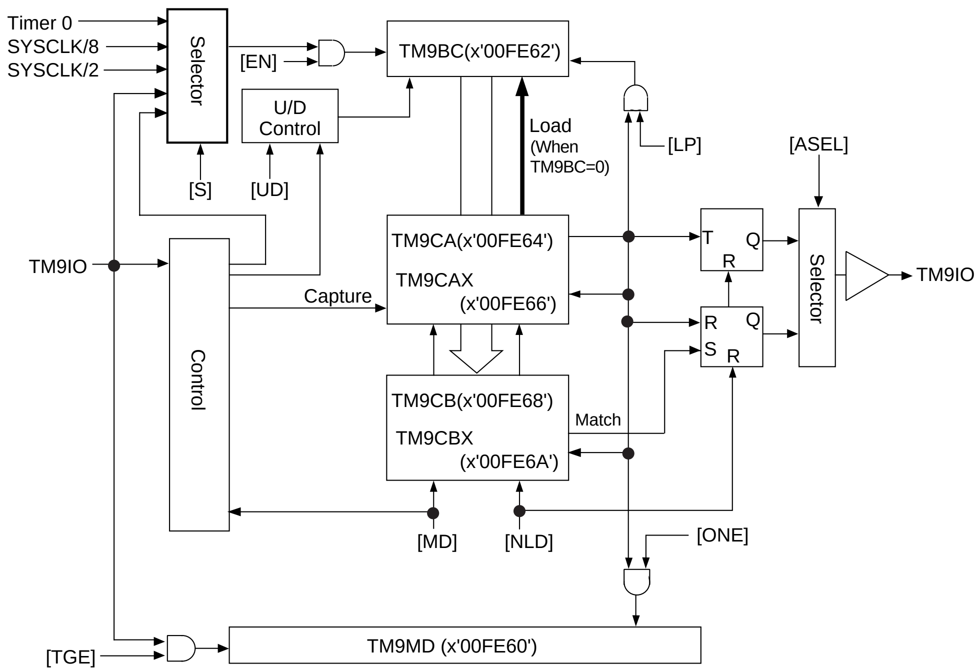


Figure 4-1-18 Timer 9 Block Diagram

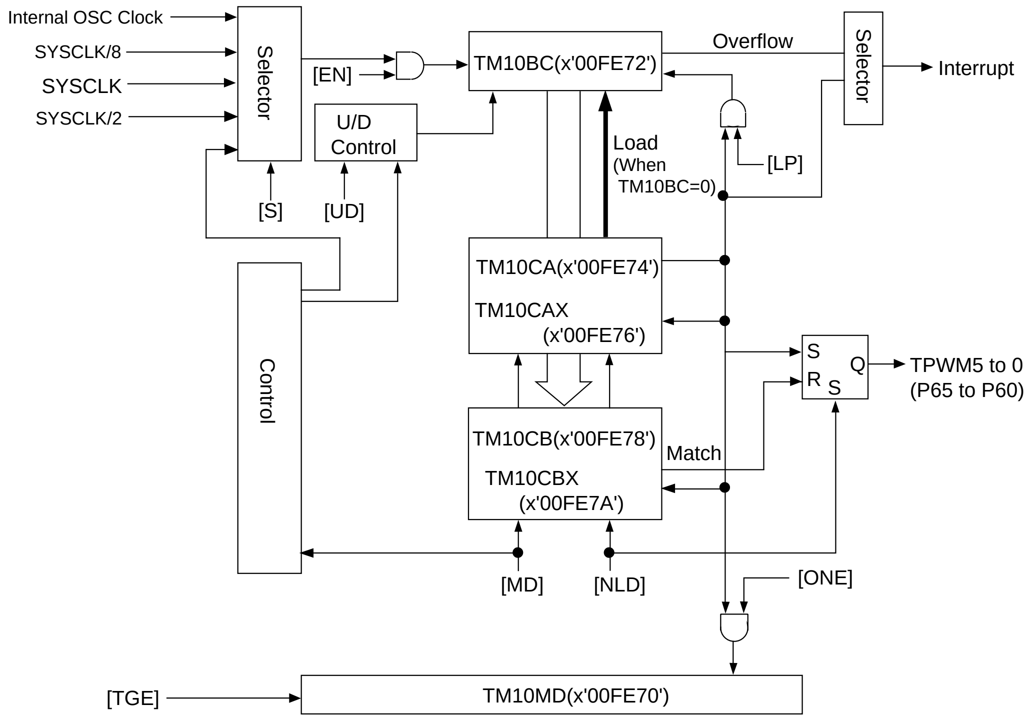


Figure 4-1-19 Timer 10 Block Diagram

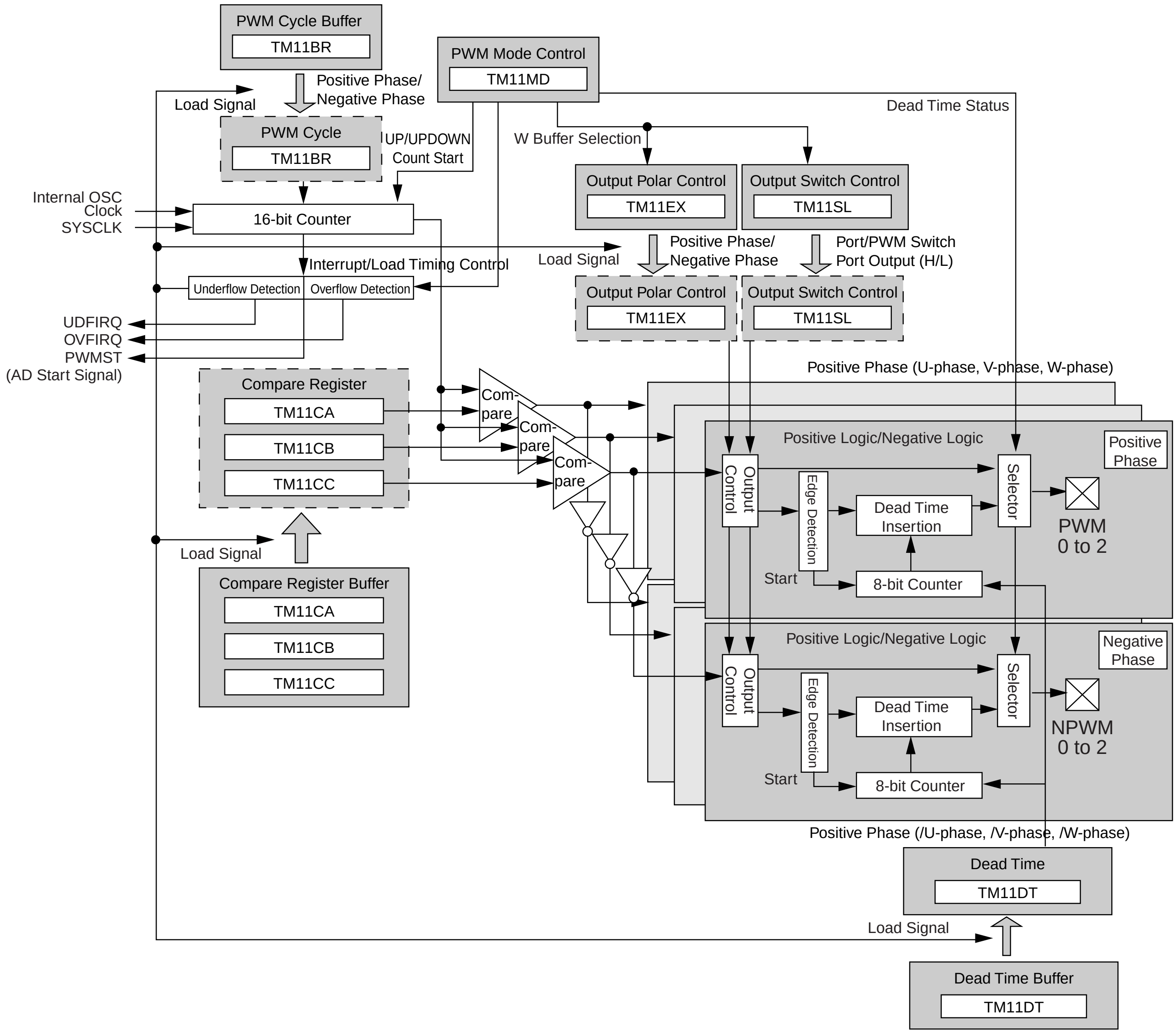


Figure 4-1-20 Timer 11 Block Diagram

4-2 8-bit Timer (Timer 0 to Timer 5) Setup Examples

4-2-1 Event Counter Using 8-bit Timer

The event counter setup procedures for Timer 0 to Timer 2 are the same. In this example, timer 2 counts the rising edge of the TM2IO pin input four times and generates an interrupt at underflow.

(1) Set P12 of port 1 as TM2IO pin by multi-port selection register (PMSEL). (Set PMSEL5 to ‘0’.)

PMSEL: x’00FFA0’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	PM SEL11	PM SEL10	PM SEL9	PM SEL8	PM SEL7	PM SEL6	PM SEL5	PM SEL4	PM SEL3	PM SEL2	PM SEL1	PM SEL0
				0	0	0	0	0	0	0	0	0	0	0	0

(2) Set the interrupt enable flag (IE) of the processor status word (PSW) to ‘1’.

This verification is unnecessary right after a reset.

(3) Verify that counting is stopped using the timer 2 mode register (TM2MD).

TM2MD: x’00FE22’

7	6	5	4	3	2	1	0
TM2 EN	TM2 LD	—	—	—	—	TM2 S1	TM2 S0
0	0	-	-	-	-	0	0

(4) Enable interrupts. At the same time, clear all prior interrupt requests. Set G3LV[2:0] bits of the maskable interrupt control register 3 (G3ICR) to the interrupt level of 6 to 0, TM2IR and TM2IE to 0 and 1, respectively. For example, write x’4200’ to the G3ICR register. Thereafter, an interrupt occurs when timer 2 underflows.

G3ICR: x’00FC46’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	G3 LV2	G3 LV1	G3 LV0	—	SC0 IE	TM2 IE	TM1 IE	—	SC0 IR	TM2 IR	TM1 IR	—	SC0 ID	TM2 ID	TM1 ID
-	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

(5) Set the timer divisor. Since timer 2 divides the TM2IO pin by 4, set the timer 2 base register (TM2BR) to ‘3’. (The valid range for TM2BR is 1 to 255.)

TM2BR: x’00FE12’

7	6	5	4	3	2	1	0
TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0
0	0	0	0	0	0	1	1

(6) Load the TM2BR value to the TM2BC register. To do this, set TM2LD and TM2EN of the TM2MD register to ‘1’ and ‘0’ respectively. At the same time, select the clock source. Set TM2S[1:0] to ‘00’.

Changing the clock source while controlling count operation will corrupt the binary counter value.

(7) Set both TM2LD and TM2EN of the TM2MD register to ‘0’. If this setting is omitted, the timer 2 binary counter may not start at the first cycle.

(8) Set both TM2LD and TM2EN to ‘0’. This makes timer 2 start. Counting starts at the beginning of the next cycle.

When the timer 2 binary counter (TM2BC) value reaches ‘0’, as soon as it loads the value of ‘3’ from the timer 2 base register (TM2BR) at the next count, a timer 2 underflow (interrupt request) occurs.

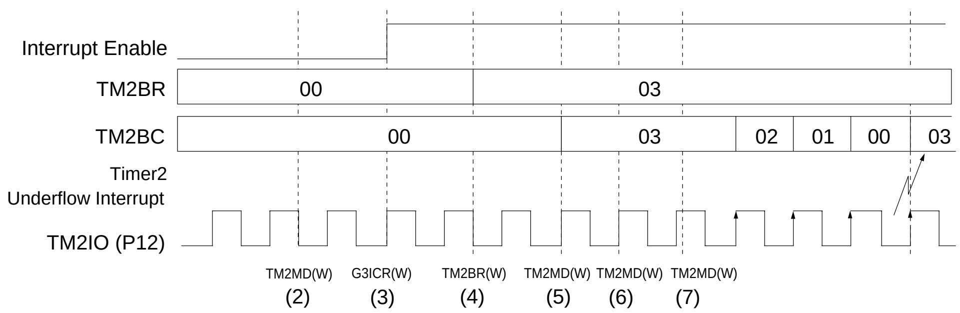


Figure 4-2-1 Event Counter Timing

4-2-2 Clock Output Using 8-bit Timer

Timer 0 to timer 2 contain clock output functions. The setup procedures for timer 0 to timer 2 are same. In this example, timer 0 and timer 1 output 12 clock cycles (SYSCLK/6).

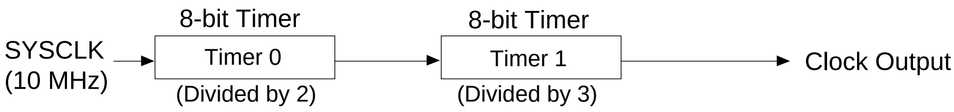


Figure 4-2-2 Clock Output Configuration (1)

■ Timer 0 Setup

This verification is unnecessary right after a reset.

(1) Verify that timer 0 counting is stopped using the timer 0 mode register (TM0MD).

TM0MD: x'00FE20'

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	—	—	—	—	TM0 S1	TM0 S0
0	0					1	0

If setting 1 of divisor, write the dummy value (for example, x'0F') once.

(2) Set the timer 0 divisor. Since timer 0 divides SYSCLK by 2, set the timer 0 base register (TM0BR) to '1'. (The valid range for TM0BR is 1 to 255.)

TM0BR: x'00FE10'

7	6	5	4	3	2	1	0
TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0
0	0	0	0	0	0	0	1

(3) Load the TM0BR value to TM0BC. To do this, set TM0LD and TM0EN to '1' and '0' respectively.

TM0MD: x'00FE20'

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	—	—	—	—	TM0 S1	TM0 S0
0	1					1	0

(4) Set both TM0LD and TM0EN of the TM0MD register to '0'. If this setting is omitted, the timer 0 binary counter may not start at the first cycle.

(5) Set TM0LD and TM0EN to ‘0’ and ‘1’ respectively. This makes timer 0 start. Counting starts at the beginning of the next cycle. When the timer 0 binary counter value reaches ‘0’, as soon as it loads the value of ‘1’ from the timer 0 base register (TM0BR) at the next count, a timer 0 underflow (interrupt request) occurs.

If selecting ‘1’ for divisor, set the dividing value ‘0’ of timer 0 to the timer 0 base register (TM0BR) once again after step (5). The first count is the value set in step (2), but after the second count it becomes ‘1’. For example, if ‘0’ is set to TM0BR in step (2), the first count is ‘257’ and the second count becomes ‘1’.

■ Pins Setup

(6) Use P11 of port 1 as TM1IO pin. Connect output of TM1IO pin to port P11 by multi-port selection register (PMSEL).

PMSEL: x’00FFA0’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	PM SEL11	PM SEL10	PM SEL9	PM SEL8	PM SEL7	PM SEL6	PM SEL5	PM SEL4	PM SEL3	PM SEL2	PM SEL1	PM SEL0
				0	0	0	0	0	0	0	0	0	0	0	0

Set TM1IO pin to output by port 1 I/O control register (P1DIR) and port 1 output mode register A (P1MDA). (Rated value is ‘2’ and ‘4’, respectively.)

P1DIR: x’00FFE1’

7	6	5	4	3	2	1	0
—	P1 DIR6	P1 DIR5	P1 DIR4	P1 DIR3	P1 DIR2	P1 DIR1	P1 DIR0
-	0	0	0	0	0	1	0

P1MDA: x’00FFF2’

7	6	5	4	3	2	1	0
—	P1MD A6	—	P1MD A4	—	P1MD A2	—	P1MD A0
-	0	-	0	-	1	-	0

■ Timer 1 Setup

(7) Verify that timer 1 counting is stopped using the timer 1 mode register (TM1MD).

This verification is unnecessary immediately after a reset.

TM1MD: x’00FE21’

7	6	5	4	3	2	1	0
TM1 EN	TM1 LD	—	—	—	—	TM1 S1	TM1 S0
0	0					1	0

(8) Set the timer 1 divisor. Since timer 1 divides timer 0 output by 3, set the timer 1 base register (TM1BR) to ‘2’. (The valid range for TM1BR is 1 to 255.)

TM1BR: x’00FE11’

7	6	5	4	3	2	1	0
TM1 BR7	TM1 BR6	TM1 BR5	TM1 BR4	TM1 BR3	TM1 BR2	TM1 BR1	TM1 BR0
0	0	0	0	0	0	1	0

Changing the clock source while controlling count operation will corrupt the binary counter value.

(9) Load the TM1BR value to TM1BC. To do this, set TM1LD and TM1EN to ‘1’ and ‘0’ respectively. At the same time, select the clock source.

(10) Set both TM1LD and TM1EN of the TM1MD register to 0. If this setting is omitted, the timer 0 binary counter may not start at the first cycle.

(11) Set TM1LD and TM1EN to ‘0’ and ‘1’ respectively. This makes timer 1 start. Counting starts at the beginning of the next cycle.

When the timer 1 binary counter (TM1BC) value reaches ‘0’, TM1IO output is inverted as soon as the value of 2 from the timer 1 base register (TM1BR) is loaded at the next count. Right after TM1BC starts counting, the TM1IO output pin outputs 0. The TM1IO output pin outputs 1 at the beginning of the next cycle when TM1BC becomes 0. Then the TM1IO output pin outputs 0 again at the beginning of the next cycle. This repeated operation realizes the clock output of 12 cycles.

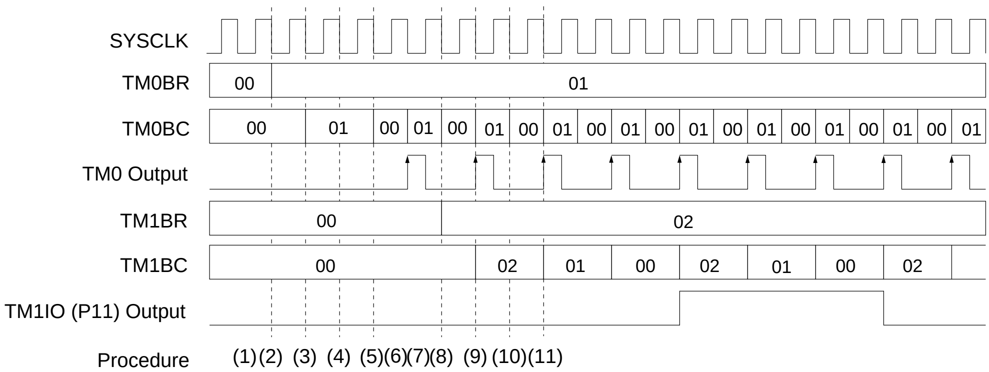


Figure 4-2-3 Clock Output Timing

4-2-3 Interval Timer Using 8-bit Timer

The interval timer setup procedures for timer 0 to timer 5 are the same. In this example, timer 0, timer 4 and timer 5 generate an interrupt at regular intervals (1 second). (To divide SYSCLK by 10,000,000, timer 0 divides SYSCLK by 250 and timer 4 and timer 5 divide SYSCLK by 40,000.)

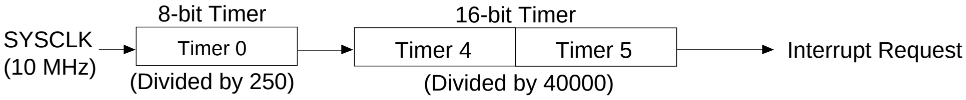


Figure 4-2-4 Clock Output Configuration (2)

(1) Set the interrupt enable flag (IE) of the processor status word (PSW) to ‘1’.

(2) Enable interrupts. At the same time, clear all prior interrupt requests. Set G4LV[2:0] bits of the maskable interrupt control register 4 (G4ICR) to the interrupt level of 6 to 0, TM3IR and TM3IE to ‘0’ and ‘1’, respectively. For example, write x’4100’ to the G4ICR register. Thereafter, an interrupt occurs when timer 3 underflows.

G4ICR: x’00FC48’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	G4 LV2	G4 LV1	G4 LV0	—	SC1 IE	TM8 IE	TM3 IE	—	SC1 IR	TM8 IR	TM3 IR	—	SC1 ID	TM8 ID	TM3 ID
-	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

■ Timer 0 Setup

(3) Verify that timer 0 counting is stopped using the timer 0 mode register (TM0MD).

This verification is unnecessary right after a reset.

TM0MD: x’00FE20’

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	—	—	—	—	TM0 S1	TM0 S0
0	0					1	0

(4) Set the timer 0 divisor. Since timer 0 divides SYSCLK by 250, set the timer 0 base register (TM0BR) to ‘249’. (The valid range for TM0BR is 1 to 255.)

If setting 1 for divisor, write the dummy value (for example, x’0F’) once.

TM0BR: x’00FE10’

7	6	5	4	3	2	1	0
TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0
1	1	1	1	1	0	0	1

(5) Load the TM0BR value to TM0BC. To do this, set TM0LD and TM0EN to '1' and '0' respectively.

TM0MD: x'00FE20'

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	—	—	—	—	TM0 S1	TM0 S0
0	0					1	0

Only when divisor is '1', set the dividing value '0' of timer 0 to the timer 0 base register (TM0BR) once again after step (7). The first count is the value set in step (4), but after the second count it becomes '1'. For example, if '0' is set to TM0BR in step (4), the first count is '257' and the second count becomes '1'.

(6) Set both TM0LD and TM0EN of the TM0MD register to '0'. If this setting is omitted, the timer 0 binary counter may not start at the first cycle.

(7) Set TM0LD and TM0EN to '0' and '1' respectively. This starts timer 0. Counting starts at the beginning of the next cycle. When the timer 0 binary counter (TM0BC) reaches 0, as soon as it loads the value of '1' from the timer 0 base register (TM0BR) at the next count, a timer 0 underflow (interrupt request) occurs.

■ Timer 4 and Timer 5 Setup

This verification is unnecessary right after a reset.

(8) Verify that counting is stopped using the timer 4 mode register (TM4MD) and the timer 5 mode register (TM5MD).

(They can be set simultaneously by 16-bit access.)

TM4MD: x'00FE24'

7	6	5	4	3	2	1	0
TM4 EN	TM4 LD	—	—	—	—	TM4 S1	TM4 S0
0	0					1	0

TM5MD: x'00FE25'

7	6	5	4	3	2	1	0
TM5 EN	TM5 LD	—	—	—	—	TM5 S1	TM5 S0
0	0					0	1

(9) Set the timer divisor. Since the divisor is 40,000 (x'9C40'), set the timer 4 base register (TM4BR) and the timer 5 base register (TM5BR) to x'3F' and x'9C' respectively. (The valid range is 1 to 255.)

TM4BR: x'00FE14'

7	6	5	4	3	2	1	0
TM4 BR7	TM4 BR6	TM4 BR5	TM4 BR4	TM4 BR3	TM4 BR2	TM4 BR1	TM4 BR0
0	0	1	1	1	1	1	1

TM5BR: x'00FE15'

7	6	5	4	3	2	1	0
TM5 BR7	TM5 BR6	TM5 BR5	TM5 BR4	TM5 BR3	TM5 BR2	TM5 BR1	TM5 BR0
1	0	0	1	1	1	0	0

(10) Load TM4BR value and TM5BR value to TM4BC and TM5BC respectively. To do this, set both TM4LD and TM5LD to ‘1’, and both TM4EN and TM5EN to ‘0’. At the same time, select clock source (timer 0 for timer 4, timer 4 cascade for timer 5).
(They can be set simultaneously by 16-bit access.)

(11) Set all TM4LD, TM5LD, TM4EN and TM5EN to ‘0’. If this setting is omitted, the binary counter may not start at the first cycle.
(They can be set simultaneously by 16-bit access.)

(12) Set TM4LD and TM5LD to 0, and TM4EN and TM5EN to ‘1’. This makes the timer start. Counting starts at the beginning of the next cycle.
(They can be set simultaneously by 16-bit access.)

When the timer 4 binary counter (TM4BC) value and the timer 5 binary counter (TM5BC) value reach ‘0’, a timer 5 underflow (interrupt request) occurs as soon as the timer 4 base register (TM4BR) value x’3F’ and the timer 5 base register (TM5BR) value x’9C’ are loaded.

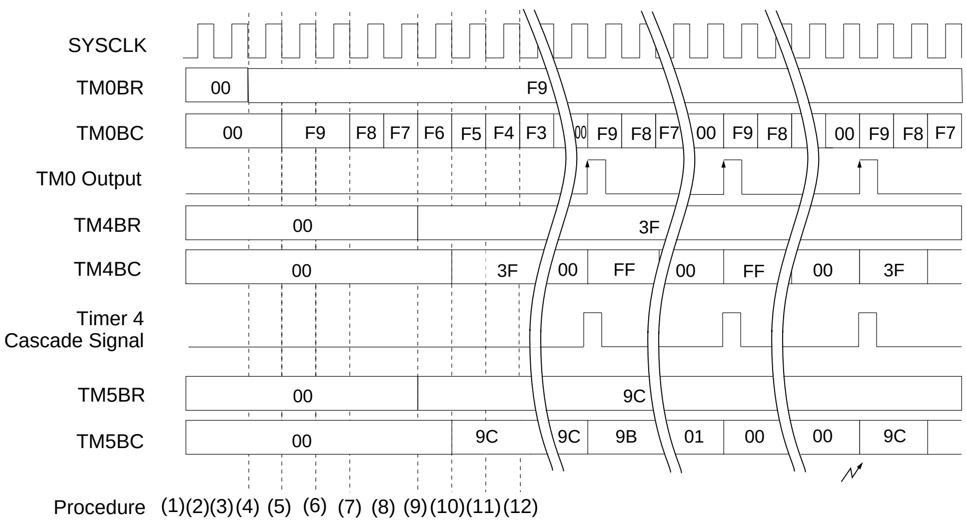


Figure 4-2-5 Interval Timer Timing

4-3 8 and 16-bit Timers (Timer 6 to Timer 10) Setup Examples

4-3-1 Event Counter Using 8 and 16-bit Timers

The event counter setup procedures for Timer 6 to Timer 9 are the same except the up/down counting selection. In this example, timer 6 counts TM6IO pin input (SYSCLK/2 or less, 5 MHz or less with 20-MHz internal oscillation) and generates an interrupt on the fifth cycle.

■ Pin Setup

(1) Set P13 of port 1 as TM6IO pin by multi-port selection register (PMSEL). (Set PMSEL6 to '0'.)

PMSEL: x'00FFA0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	PM SEL11	PM SEL10	PM SEL9	PM SEL8	PM SEL7	PM SEL6	PM SEL5	PM SEL4	PM SEL3	PM SEL2	PM SEL1	PM SEL0
				0	0	0	0	0	0	0	0	0	0	0	0

Use the MOV instruction to set the data and always use 16-bit write operations.

■ Interrupt Enable Setup

(2) Enable interrupts. At the same time, clear all prior interrupt requests. Set G6LV[2:0] bits of the G6ICR to the interrupt level of 6 to 0, TM6IR to '0', and TM6IE to '1'. For example, write x'4200' to the G4ICR register. Thereafter, an interrupt occurs when the timer 6 underflow occurs.

Stop TM6BC counting and initialize (clear) TM6BC and RS.F.F.

■ Timer 6 Setup

(3) Set the operating mode to the timer 6 mode register (TM6MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Select TM6IO as the timer 6 clock source.

TM6MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	—	—	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	—	TM6 LP	TM6 ASEL	—	TM6 S1	TM6 S0
0	0	-	-	0	1	0	0	0	0	-	1	0	-	1	0

(4) Set the timer 6 divisor. Since timer 6 divides TM6IO pin input by 5, set the timer 6 compare/capture register A (TM6CA) to ‘4’. (The valid range for TM6CA is 1 to x’FFFE’.)

TM6CA: x’00FE34’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CA15	TM6 CA14	TM6 CA13	TM6 CA12	TM6 CA11	TM6 CA10	TM6 CA9	TM6 CA8	TM6 CA7	TM6 CA6	TM6 CA5	TM6 CA4	TM6 CA3	TM6 CA2	TM6 CA1	TM6 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

(5) Set TM6NLD and TM6EN of the timer 6 mode register (TM6MD) to ‘1’ and ‘0’ respectively. This enables TM6BC, T.F.F. and RS.F.F.

In the single buffer mode, both TM6CA and TM6CB are compared to TM6BC.

The TM6CB value is set to ‘-1’ by writing x’FFFF’ to TM6CB. When TM6CB is not compared to TM6BC, the TM6CB value is set to ‘-1’.

TM6MD: x’00FE30’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	—	—	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	—	TM6 LP	TM6 ASEL	—	TM6 S1	TM6 S0
0	1	-	-	0	1	0	0	0	0	-	1	0	-	1	0

(6) Set both TM6NLD and TM6EN to ‘1’. This makes the timer 6 start. Counting starts at the beginning of the next cycle.

If this step is omitted, TM6BC may not count during the first cycle. Do not change other bits in the TM6MD register at the same time.

When SYSCLK operates (in normal and halt modes), the external TM6IO input is sampled on SYSCLK. When SYSCLK stops (in STOP mode), TM6BC counts the TM6IO input. Select the oscillation clock/4 (5 MHz with an internal 20-MHz oscillator) or less as the event counter clock.
Figure 4-3-1 shows the example of generating an interrupt during up counting.

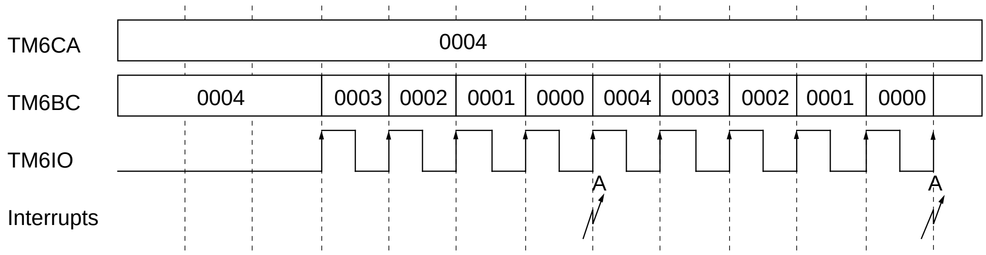


Figure 4-3-1 Event Counter Timing

4-3-2 PWM Output Using 8 and 16-bit Timers

The PWM output setup procedures for Timer 6 to Timer 9 are the same except the up/down counting selection. In this example, timer 6 divides SYSCLK by 5 and outputs PWM signal on the fifth cycle. The duty is 2:3. Therefore, set the divisor of 5 (the set value is '4') to the timer 6 compare/capture register A and the cycle of 2 (the set value is '1') to the timer 6 compare/capture B.

■ Pin Setup

(1) Use P13 of port 1 as TM6IO pin. Connect output of TM6IO pin to port P13 by multi-port selection register (PMSEL). (Set PMSEL6 to '0'.)

PMSEL: x'00FFA0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	PM SEL11	PM SEL10	PM SEL9	PM SEL8	PM SEL7	PM SEL6	PM SEL5	PM SEL4	PM SEL3	PM SEL2	PM SEL1	PM SEL0
				0	0	0	0	0	0	0	0	0	0	0	0

Set the TM6IO pin to output by using the port 1 I/O control register (P1DIR) and the port 1 output mode register A (P1MDA).

P1DIR: x'00FFE1'

7	6	5	4	3	2	1	0
—	P1 DIR6	P1 DIR5	P1 DIR4	P1 DIR3	P1 DIR2	P1 DIR1	P1 DIR0
-	0	0	0	1	0	0	0

P1MDA: x'00FFF2'

7	6	5	4	3	2	1	0
—	P1MD A6	—	P1MD A4	—	P1MD A2	—	P1MD A0
-	1	-	0	-	0	-	0

Use the MOV instruction to set the data and always use 16-bit write operations.

Stop TM6BC counting and initialize (clear) TM6BC and RS.F.F.

■ Timer 6 Setup

(2) Set the operating mode to the timer 6 mode register (TM6MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Select SYSCLK as the timer 6 clock source. Select the double buffer for operating mode.

TM6MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	—	—	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	—	TM6 LP	TM6 ASEL	—	TM6 S1	TM6 S0
0	0	-	-	0	0	0	0	0	1	-	1	0	-	1	1

(3) Set the timer 6 divisor. Since timer 6 divides SYSCLK by 5, set the timer 6 compare/capture register A (TM6CA) to ‘4’. (The valid range for TM6CA is 1 to x’FFFE’.)

TM6CA: x’00FE34’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CA15	TM6 CA14	TM6 CA13	TM6 CA12	TM6 CA11	TM6 CA10	TM6 CA9	TM6 CA8	TM6 CA7	TM6 CA6	TM6 CA5	TM6 CA4	TM6 CA3	TM6 CA2	TM6 CA1	TM6 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

(4) Set the timer 6 duty. Since the duty is 2/5 of SYSCLK, set the timer 6 compare/capture register B (TM6CB) to ‘1’. (The valid range for TM6CB is -1 ≤ TM6CB < TM6CA.)

The TM6CB value is set to ‘-1’ by writing x’FFFF’ to TM6CB. When TM6CB is not compared to TM6BC, the TM6CB value is set to ‘-1’.

TM6CB: x’00FE38’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CB15	TM6 CB14	TM6 CB13	TM6 CB12	TM6 CB11	TM6 CB10	TM6 CB9	TM6 CB8	TM6 CB7	TM6 CB6	TM6 CB5	TM6 CB4	TM6 CB3	TM6 CB2	TM6 CB1	TM6 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(5) In the double buffer mode, TM6BC is compared to TM6CAX. TM6CAX remains x’0000’ before TM6BC starts counting because the TM6CAX is updated when TM6CAX = TM6BC. Therefore, to load the TM6CA value to TM6CAX, write the dummy data to TM6CAX. (The dummy data can be any values.)

TM6CAX and TM6CBX are valid only when the timer 6 compare/ capture register is set to double buffer mode.

TM6CAX: x’00FE36’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CAX15	TM6 CAX14	TM6 CAX13	TM6 CAX12	TM6 CAX11	TM6 CAX10	TM6 CAX9	TM6 CAX8	TM6 CAX7	TM6 CAX6	TM6 CAX5	TM6 CAX4	TM6 CAX3	TM6 CAX2	TM6 CAX1	TM6 CAX0

(6) In the double buffer mode, TM6BC is compared to TM6CBX. TM6CBX remains x’0000’ before TM6BC starts counting because the TM6CBX is updated when TM6CBX = TM6BC. Therefore, to load the TM6CA value to TM6CBX, write the dummy data to TM6CBX. (The dummy data can be any values.)

TM6CBX: x’00FE3A’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CBX15	TM6 CBX14	TM6 CBX13	TM6 CBX12	TM6 CBX11	TM6 CBX10	TM6 CBX9	TM6 CBX8	TM6 CBX7	TM6 CBX6	TM6 CBX5	TM6 CBX4	TM6 CBX3	TM6 CBX2	TM6 CBX1	TM6 CBX0

The setup steps after step (6) are the same as steps (5) and (6) in ‘4-3-1 Event Counter Using 8 and 16-bit Timers’.

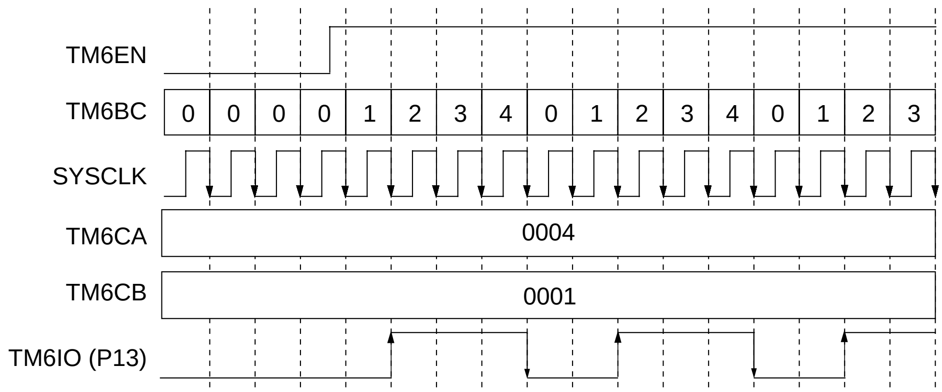


Figure 4-3-2 PWM Timing

When timer n changes the duty of PWM output waveforms dynamically, the PWM output waveforms may corrupt depending on the timing of changing the TMnCB value in the single buffer mode. In the double buffer mode, the corruption of PWM output waveforms does not occur at any timing of changing the TMnCB value. This corruption does not occur even when the output waveforms consist of 1s and 0s.

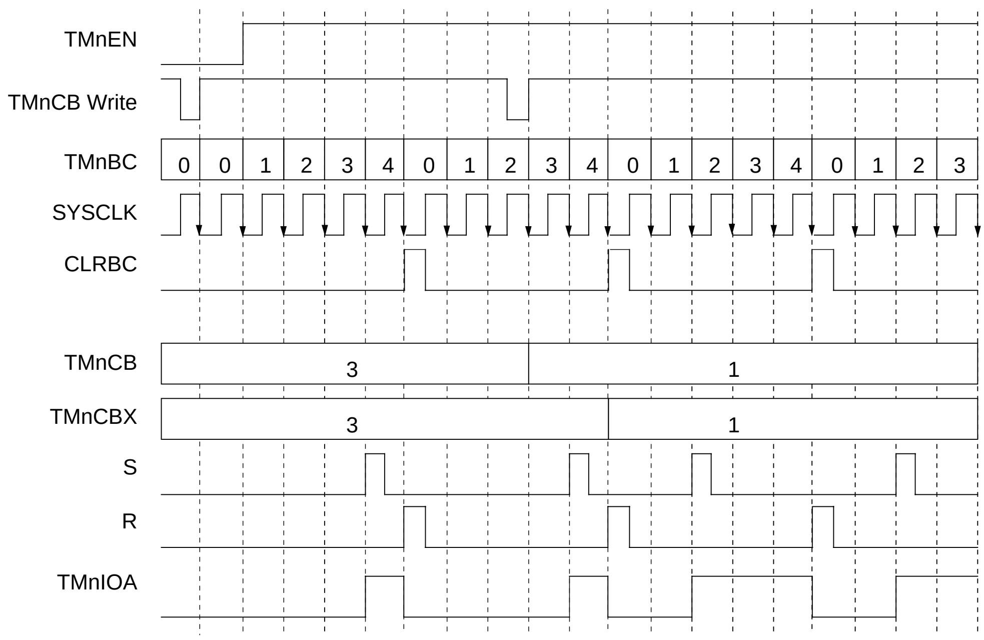


Figure 4-3-3 PWM Timing in Double Buffer Mode

4-3-3 One-phase Capture Input Using 8 and 16-bit Timers

The one-phase capture input setup procedures for Timer 6 to Timer 9 are the same except the up/down counting selection. In this example, timer 7 divides SYSCLK by 65536 and measures the width of 1 interval of TM7IO pin input. The width can be measured by calculating (TMnCB-TMnCA) with software.

■ Pin Setup

(1) Set P14 of port 1 as TM7IO pin by multi-port selection register (PMSEL). (Set PMSEL7 to '0'.)

Use the MOV instruction to set the data and always use 16-bit write operations.

PMSEL: x'00FFA0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	PM SEL11	PM SEL10	PM SEL9	PM SEL8	PM SEL7	PM SEL6	PM SEL5	PM SEL4	PM SEL3	PM SEL2	PM SEL1	PM SEL0
				0	0	0	0	0	0	0	0	0	0	0	0

■ Timer 7 Setup

(2) Set the operating mode to the timer 7 mode register (TM7MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Set TM7LP to '0' and count 0 to x'FFFF' repeatedly. Select SYSCLK as the timer 7 clock source.

Stop TM7BC counting and initialize (clear) TM7BC and RS.F.F.

TM7MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7 NLD	—	—	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	—	TM7 LP	TM7 ASEL	—	TM7 S1	TM7 S0
0	0	-	-	0	0	0	0	1	0	-	0	0	-	1	1

(3) Set TM7NLD to '1' and TM7En to '0'. This enables TM7BC, T.F.F. and RS.F.F. Do not change other bits in the TM7MD register at the same time.

If this step is omitted, TM7BC may not count during the first cycle.

(4) Set both TM7NLD and TM7EN to '1'. This makes the timer 7 start. Counting starts at the beginning of the next cycle.

■ Compare/Capture Register Setup

(5) When TM7MDn = ‘10’ (the capture is selected), TM7CA and TM7CB are reserved for read operations. When setting TM7CA and TM7CB is required, first set TM7MDn to ‘00’.

TM7CA: x’00FE44’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CA15	TM7 CA14	TM7 CA13	TM7 CA12	TM7 CA11	TM7 CA10	TM7 CA9	TM7 CA8	TM7 CA7	TM7 CA6	TM7 CA5	TM7 CA4	TM7 CA3	TM7 CA2	TM7 CA1	TM7 CA0

TM7CB: x’00FE48’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CB15	TM7 CB14	TM7 CB13	TM7 CB12	TM7 CB11	TM7 CB10	TM7 CB9	TM7 CB8	TM7 CB7	TM7 CB6	TM7 CB5	TM7 CB4	TM7 CB3	TM7 CB2	TM7 CB1	TM7 CB0

TM7CA is captured on the rising edge of TM7IO, and TM7CB is captured on the falling edge of TM7IO.

Load the TM7CA value and TM7CB value during interrupt processing.

The width is calculated by ignoring flags even though the TM7CA value is greater than the TM7CB value.

■ Width Calculation

(6) Calculate the width. Store the TM7CA value and TM7CB value to the data register and subtract TM7CA from TM7CB. Ignore C and V flags. The width is calculated correctly by setting TM7LP to 0 even though the TM7CA value is greater than the TM7CB value. The following figure shows 000A - 0007 = 0003 or 3 cycles.

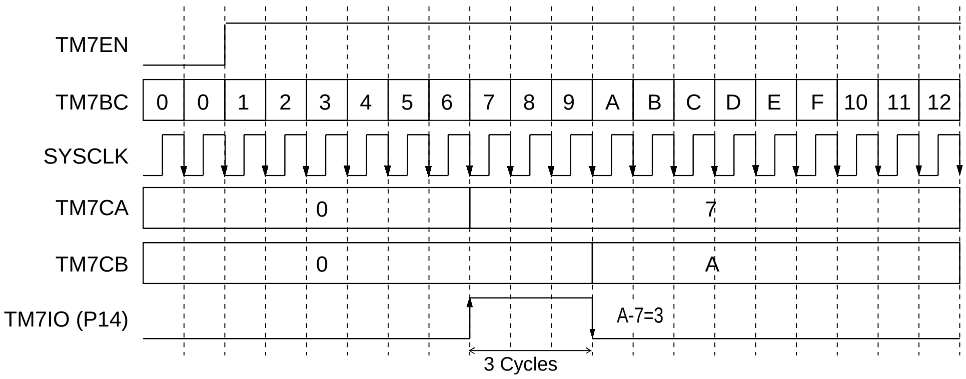


Figure 4-3-4 One-phase Capture Timing

4-3-4 External Count Direction Control Using 8 and 16-bit Timers

The external count direction control setup procedures for timer 6 to timer 9 are the same. In this example, timer 7 counts SYSCLK and controls the counting direction (up/down) using TM7IO.

■ Pin Setup

(1) Set P14 of port 1 as TM7IO pin by multi-port selection register (PMSEL). (Set PMSEL7 to ‘0’.)

Use the MOV instruction to set the data and always use 16-bit write operations.

PMSEL: x’00FFA0’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	PM SEL11	PM SEL10	PM SEL9	PM SEL8	PM SEL7	PM SEL6	PM SEL5	PM SEL4	PM SEL3	PM SEL2	PM SEL1	PM SEL0
				0	0	0	0	0	0	0	0	0	0	0	0

■ Timer 7 Setup

(2) Set the operating mode to the timer 7 mode register (TM7MD). Verify that counting is stopped and an interrupt is disabled. The count direction is up when TM7IO pin is ‘1’ while the count direction is down when TM7IO is ‘0’. Select SYSCLK as the timer 7 clock source.

Stop TM7BC counting and initialize (clear) TM7BC and RS.F.F.

(3) When TM7CA is used for looping, set the timer 7 looping value (the valid range is 1 to x’FFFF’). When writing x’1FFF’ to TM7CA, the TM7BC counts from 0 to x’1FFF’.

TM7MD: x’00FE40’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7 NLD	—	—	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	—	TM7 LP	TM7 ASEL	—	TM7 S1	TM7 S0
0	0	-	-	1	0	0	0	0	0	-	1	0	-	1	1

(4) Set TM7NLD to ‘1’ and TM7EN to ‘0’. This enables TM7BC, T.F.F. and RS.F.F.

If this step is omitted, TM7BC may not count during the first cycle.

(5) Set both TM7NLD and TM7EN to ‘1’. This makes the timer 7 start. Counting starts at the beginning of the next cycle.

Timer 7 controls the count direction by using TM7IO. The count direction becomes the opposite edge of the count edge (shown as ○ in Figure 4-3-5). Figure 4-3-5 shows the external count direction control timing and the example of becoming down counting from up counting.

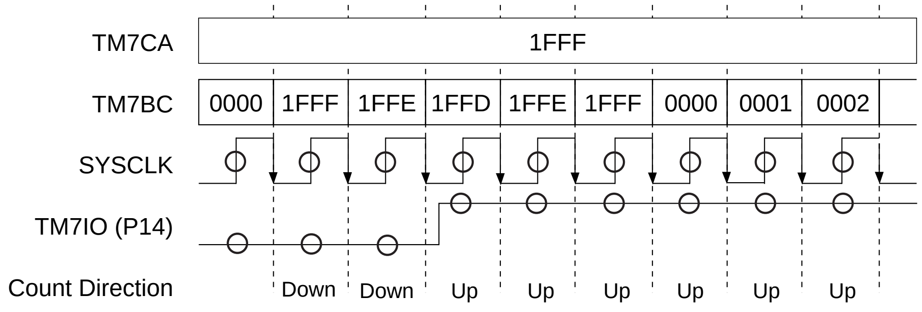


Figure 4-3-5 External Count Direction Control Timing

4-3-5 Simplified Six-phase PWM Output by 8-bit Timer (Timer 10)

In this example, timer 10 divides SYSCLK by 5 and outputs six-phase PWM signal on the fifth cycle. The duty is 2:3. Therefore, set the divisor of 5 (the set value is '4') to the timer 10 compare/capture register A, and the cycle of 2 (the set value is '1') to the timer 10 compare/capture register B.

■ Pin Setup

(1) Set the TPWM0 to 5 pins to output by using the port 6 I/O control register (P6DIR), the port 6 output mode register A (P6MDA) and the port 6 output mode register B (P6MDB).

P6DIR: x'00FFE8'

7	6	5	4	3	2	1	0
—	—	P6 DIR5	P6 DIR4	P6 DIR3	P6 DIR2	P6 DIR1	P6 DIR0
-	-	1	1	1	1	1	1

P6MDB: x'00FFFA'

7	6	5	4	3	2	1	0
—	—	—	—	—	—	P6MD B1	P6MD B0
-	-	-	-	-	-	0	1

P6MDA: x'00FFFB'

7	6	5	4	3	2	1	0
P6MD A7	P6MD A6	P6MD A5	P6MD A4	P6MD A3	P6MD A2	P6MD A1	P6MD A0
1	0	1	0	1	1	0	1

■ Timer 10 Setup

(2) Set the operating mode to the timer 10 mode register (TM10MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Select SYSCLK as the timer 10 clock source. Select the double buffer operating mode.

Use the MOV instruction to set the data and always use 16-bit write operations.

Stop TM10BC counting and initialize (clear) TM10BC and RS.F.F.

TM10MD: x'00FE70'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 EN	TM10 NLD	—	TM10 SEL	—	TM10 UD0	—	TM10 ONE	—	TM10 MD0	—	TM10 LP	—	—	TM10 S1	TM10 S0
0	0	-	0	-	0	-	0	-	1	-	1	-	-	1	0

(3) Set the timer 10 divisor. Since timer 10 divides SYSCLK by 5, set the timer 10 compare/capture register A (TM10CA) to '4'. (The valid range for TM10CA is 1 to x'FFFE'.)

TM10CA: x'00FE74'

7	6	5	4	3	2	1	0
TM10 CA7	TM10 CA6	TM10 CA5	TM10 CA4	TM10 CA3	TM10 CA2	TM10 CA1	TM10 CA0
0	0	0	0	0	1	0	0

The TM10CB value is set to '-1' by writing x'FFFF' to TM10CB. When TM10CB is not compared to TM10BC, the TM10CB value is set to '-1'.

(4) Set the timer 10 duty. Since the duty is 2/5 of SYSCLK, set the timer 10 compare/capture register B (TM10CB) to '1'. (The valid range for TM10CB is -1 ≤ TM10CB < TM10CA.)

TM10CB: x'00FE78'

7	6	5	4	3	2	1	0
TM10 CB7	TM10 CB6	TM10 CB5	TM10 CB4	TM10 CB3	TM10 CB2	TM10 CB1	TM10 CB0
0	0	0	0	0	0	0	1

TM10CAX and TM10CBX are valid only when the timer 10 compare/capture register is set to double buffer mode.

(5) In the double buffer mode, TM10BC is compared to TM10CAX. TM10CAX remains x'0000' before TM10BC starts counting because the TM10CAX is updated when TM10CAX = TM10BC. Therefore, to load the TM10CA value to TM10CAX, write the dummy data to TM10CAX. (The dummy data can be any values.)

TM10CAX: x'00FE76'

7	6	5	4	3	2	1	0
TM10 CAX7	TM10 CAX6	TM10 CAX5	TM10 CAX4	TM10 CAX3	TM10 CAX2	TM10 CAX1	TM10 CAX0

(6) In the double buffer mode, TM10BC is compared to TM10CBX. TM10CBX remains x'0000' before TM10BC starts counting because the TM10CBX is updated when TM10CBX = TM10BC. Therefore, to load the TM10CA value to TM10CBX, write the dummy data to TM10CBX. (The dummy data can be any values.)

TM10CBX: x'00FE7A'

7	6	5	4	3	2	1	0
TM10 CBX7	TM10 CBX6	TM10 CBX5	TM10 CBX4	TM10 CBX3	TM10 CBX2	TM10 CBX1	TM10 CBX0

The setup steps after step (6) are the same as steps (5) and (6) in '4-3-1 Event Counter Using 8 and 16-bit Timers'.

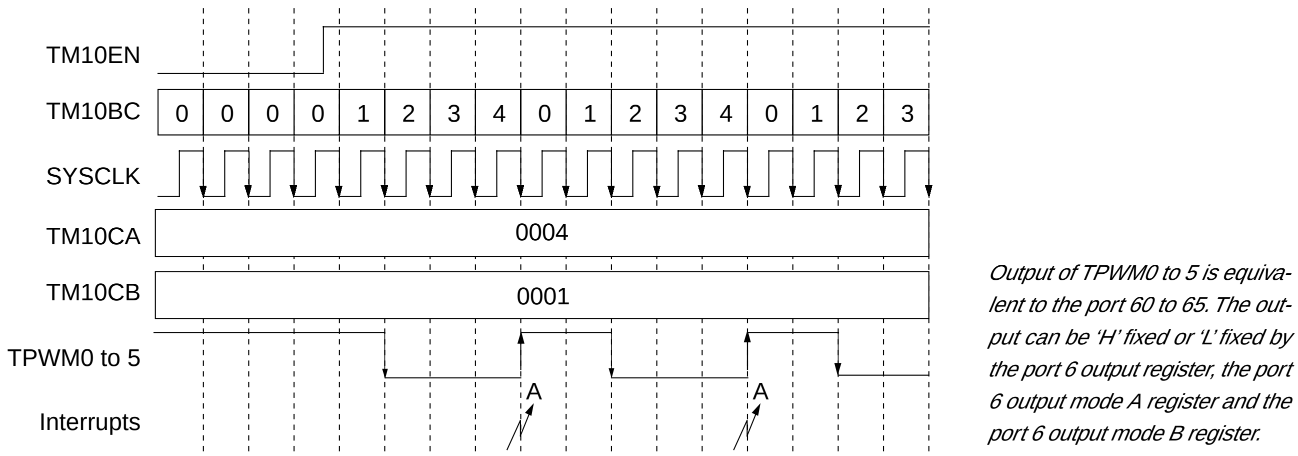


Figure 4-3-6 PWM Timing

When timer n changes the duty of PWM output waveforms dynamically, the PWM output waveforms or interrupts may corrupt at the timing of changing the TM10CB value in the single buffer mode. In the double buffer mode, the corruption of PWM output waveforms or interrupts does not occur at any timing of changing the TM10CB value. This corruption does not occur even when the output waveforms consist of 1s and 0s.

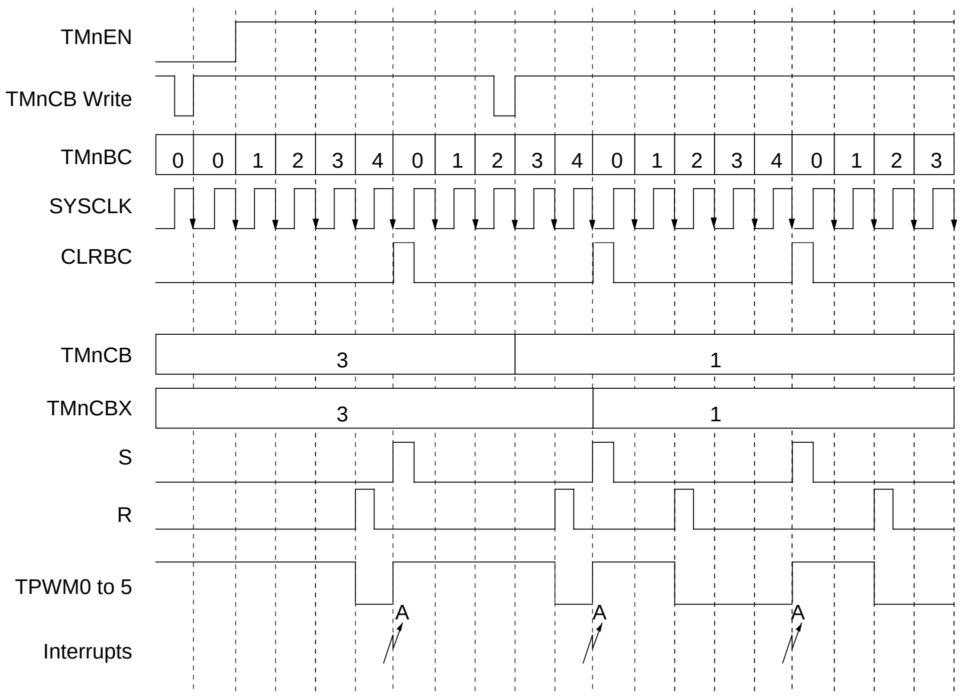


Figure 4-3-7 PWM Double Buffer Mode Timing

4-4 Six-phase PWM for Motor Control (Timer 11)

4-4-1 PWM

This LSI contains complementary three-phase PWM for motor control.

Items	Functions
PWM for motor control	There is three-phase (U-phase, V-phase and W-phase) PWM output. PWM cycle is set by 16-bit counter synchronized with the microcontroller clock. PWM pulse width can be set by the three-phase independent compare register. Regiser can be rewritten during PWM operation by double buffer. Dead time can be set.
Waveform mode setup	Set 16-bit counter, which sets PWM cycle, to up-counter or up/down conter. That sets waveform mode to saw tooth wave or triangular wave.
Dead time setup	Dead time is built-in. Dead time is set by 8-bit counter cynchronized with the microcontoller clock. PWM output during dead time can be set "L" or "H" by setting output logic. This is double buffer.
Interrupt setup	An interrupt signal can be generated at PWM cycle overflow or underflow timing.
A/D synchronization	AD conversion can be started at PWM cycle comparison agreement or underflow timing.
Inhibition of output at $\overline{\text{NMI}}$ generation	At the time when six output ports (PWM2 to 0 and $\overline{\text{PWM}}$2 to 0) are selected by the port 4 output mode registers (P4MDA and P4MDB), and bp1=1 of P4MDA register is set, if external $\overline{\text{NMI}}$ is generated, P4DIR register is forcibly gotten to be ALL'0' and six PWM output ports above become Hi-Z (inhibition of output). Inhibition of output can be released by rewriting P4DIR register after $\overline{\text{NMI}}$ interruption.

4-4-2 Waveform Mode

This PWM has triangular wave and saw tooth wave, and can output solid signal to pins without reference to PWM output.

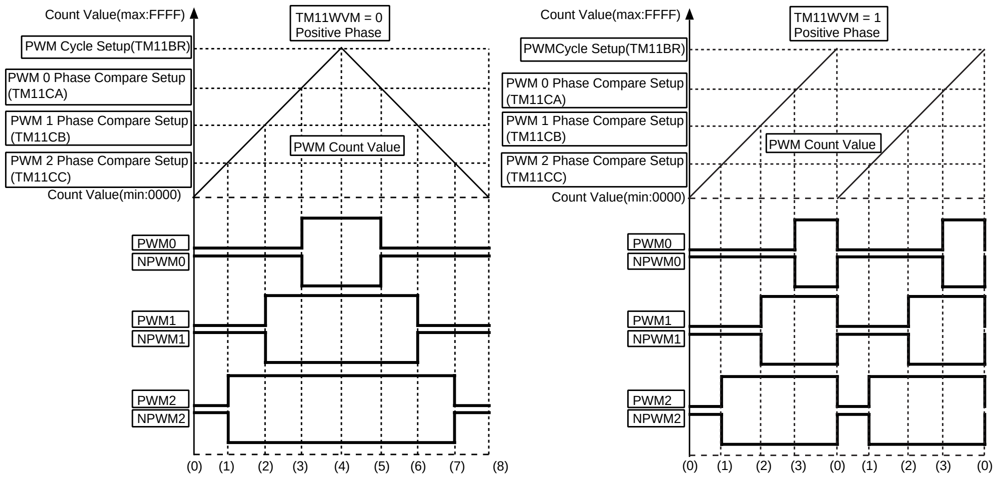


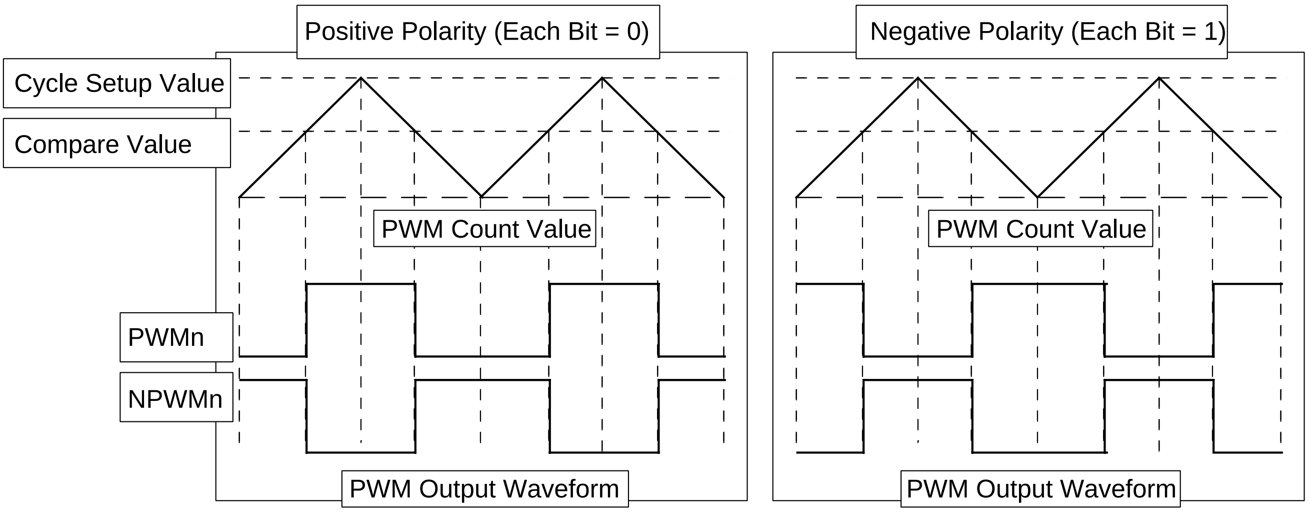
Figure 4-4-1 PWM (Timer 11) Waveform Mode

Logical operational expression of output waveform: Compare value ≤ Counter value ⇒ ‘H’
Set the counter to up/down count (triangular wave) or up-count (saw tooth wave). Triangular wave counts each the cycle setting value and 0 twice at the end of each up-count and down-count. Saw tooth wave up-counts to the cycle setting value, and gets to 0 after reaching it.
Set waveform to triangular wave or saw tooth wave. The default value is set to ‘0’ for triangular wave.

Notes to count operation
PWM block operation can be controlled at bp1:T11CEN of TM11MD.
Count is started at T11CEN=1.
The status of PWM block at count operation disable is shown below.
1) Each phase output is fixed.
When output polarity is positive. PWM0 to 2: ‘L’
NPWM0 to 2: ‘H’
When output polarity is negative. PWM0 to 2:’H’
NPWM0 to 2: ‘L’
2) 16-bit PWM cycle counter is fixed at reset.
3) The date of double buffer is directly downloaded to PWM register.
4) Dead time counter is fixed at reset after stabilization.
5) PWM control register can be read and written.
6) The date of double buffer is saved.

4-4-3 The Polarity of Output Waveform

Timer 11 output polarity control register (TM11EX) can control the polarity of PWM waveform.
When each bit is ‘1’, the signals of PWMn and NPWMn counterchange.
Setting can be done per each PWM output pair.
{PWM0, NPWM0} TM11EX bp0
{PWM1, NPWM1} TM11EX bp1
{PWM2, NPWM2} TM11EX bp2
The default value is ‘0’ of negative polarity.



4-4-4 Double Buffer

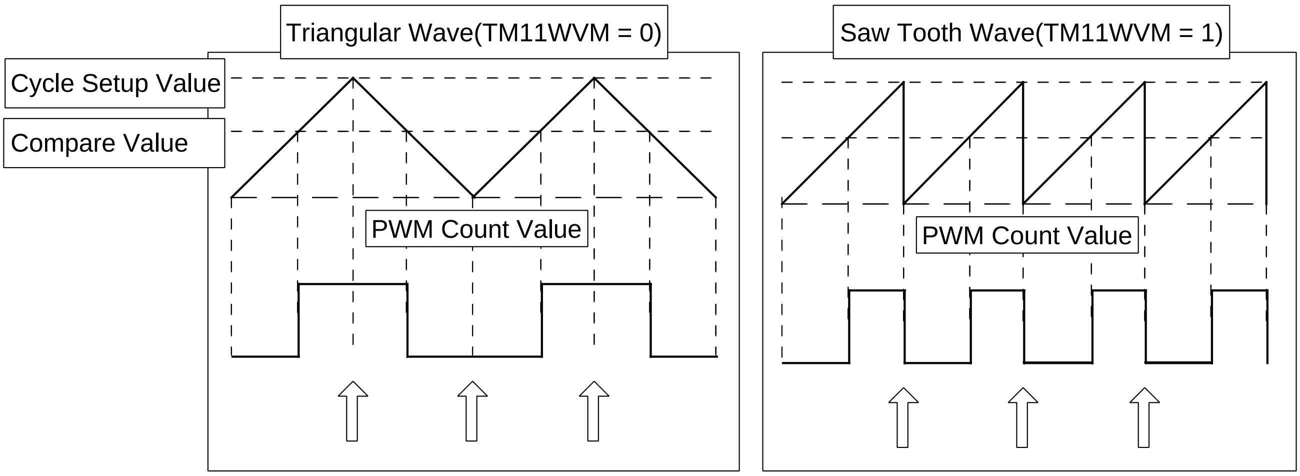
Each register for Timer 11 has double buffer so that the date can be changed during PWM operation. The register reading and writing from the microcontroller and the register referred by PWM are separated, and the register value of the microcontroller is downloaded to the register of Timer 11 at the timing synchronized with PWM cycle. The mode control register (TM11MD) for Timer11 has only single buffer because it is the basic register to control PWM operation. Except it, some control registers for Timer 11 have only double buffer and others can switch double buffer and single buffer to answer purposes. Verify each register configuration referring to Chapter 8. The load timing of double buffer can be set at two points: the timing when 16-bit Timer 11 cycle counter and Timer 11 cycle setting register match, and underflow. The permission and inhibition of load can be set with Timer 11 mode control register (TM11MD) at both timing. All double buffer of control registers is loaded at the same timing. When 16-bit Timer 11 cycle counter is not operated with counter operation disable, the value of double buffer is directly loaded to the register of Timer 11.

The table of double buffer and single buffer of Timer 11 control registers

	Double buffer	Single buffer	Remarks
TM11MD	-	√	Single only
TM11EX	√	√	Switchable Note1)
TM11SL	√	√	Switchable Note2)
TM11BR	√	-	Double only
TM11CA	√	-	Double only
TM11CB	√	-	Double only
TM11CC	√	-	Double only
TM11DT	√	-	Double only

Note 1) Switchable at bp9:TM11SDSA of TM11MD

Note 2) Switchable at bp8:TM11SDSB of TM11MD



The load timing of double buffer

bp7:TM11PCRA of TM11MD	16-bit Timer 11 cycle counter underflow 0: inhibition 1: permission
bp6:TM11PCRB of TM11MD	16-bit Timer 11 cycle counter =Timer 11 cycle setting register 0: inhibition 1: permission

Timer interrupt timing setup

The interrupt signal can be generated at the timing synchronizes with PWM cycle. The timing of interrupt signal generation can be set at two points: the timing when 16-bit Timer 11 cycle counter and Timer 11 cycle setting register match, and underflow.

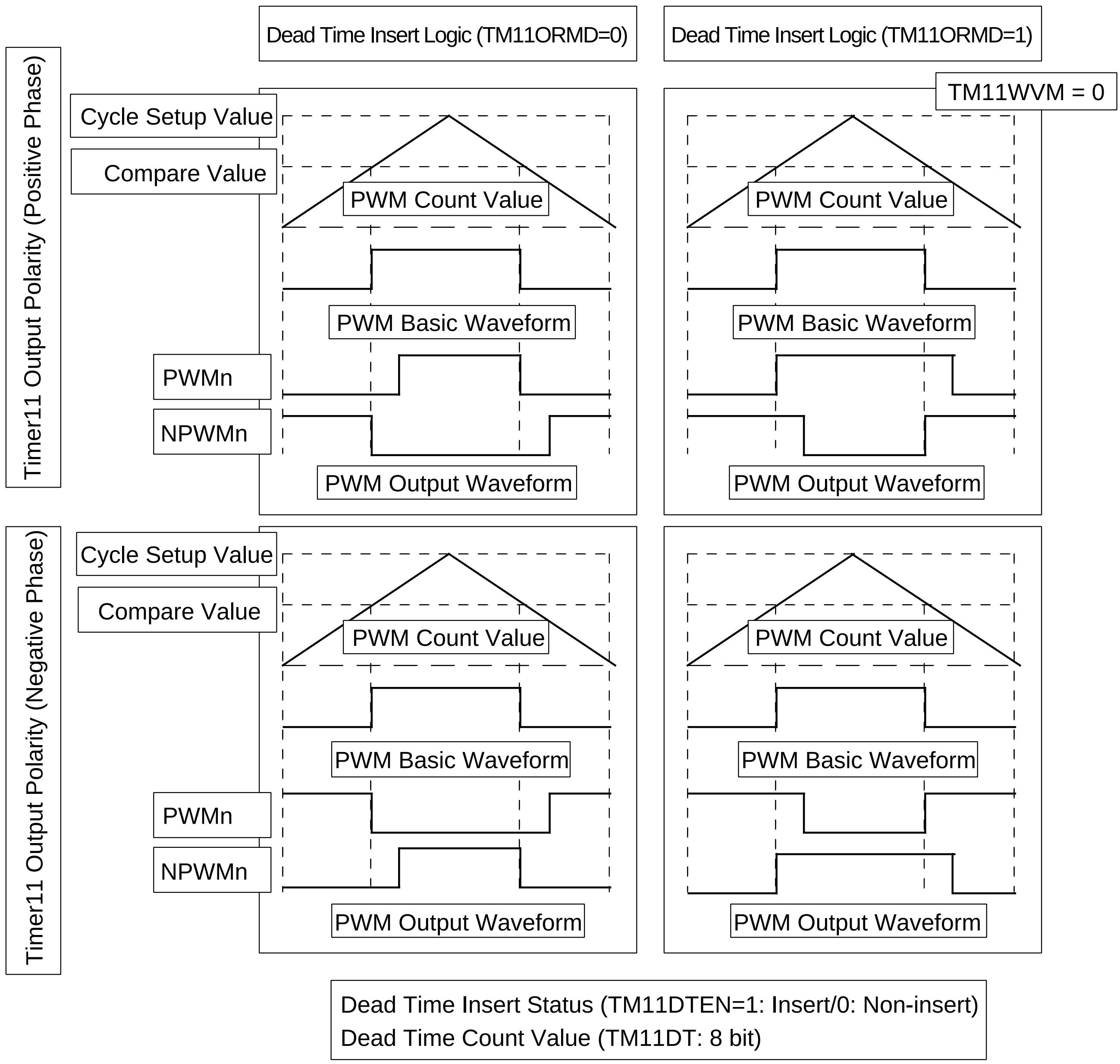
Timer interrupt timing setup

bp5:TM11INTA of TM11MD	16-bit Timer 11 cycle counter underflow 0: inhibition 1: permission
bp4:TM11INTB of TM11MD	16-bit Timer 11 cycle counter =Timer 11 cycle setting register 0: inhibition 1: permission

4-4-5 Dead Time

Dead time inserts on-time delay to up-phase and down-phase when a signal turns over at each phase of PWM output. Dead time status can be selected at bp3:TM11DTEN of TM11MD. At dead time insert, output logic can be selected at bp2:TM11ORMD of TM11MD.

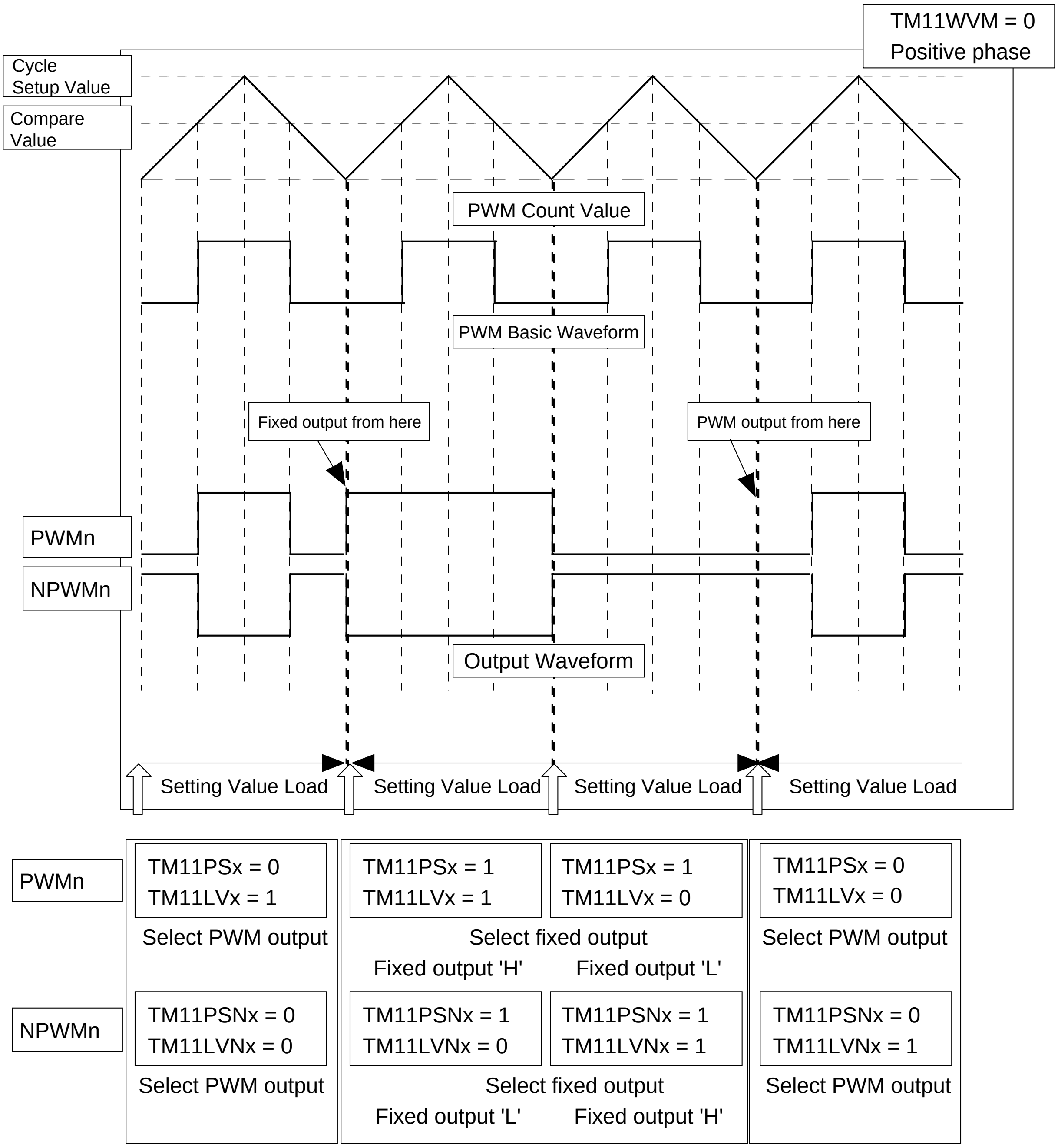
Delay time inserted at dead time is set at dead time setting register (TM11DT). Delay time can be set from 00 to FF with 8-bit data. Calculate dead time delay by setting value +1. That means when setting value is 00 with dead time, 1 clk dead time is inserted.



4-4-6 Fixed Output Setup

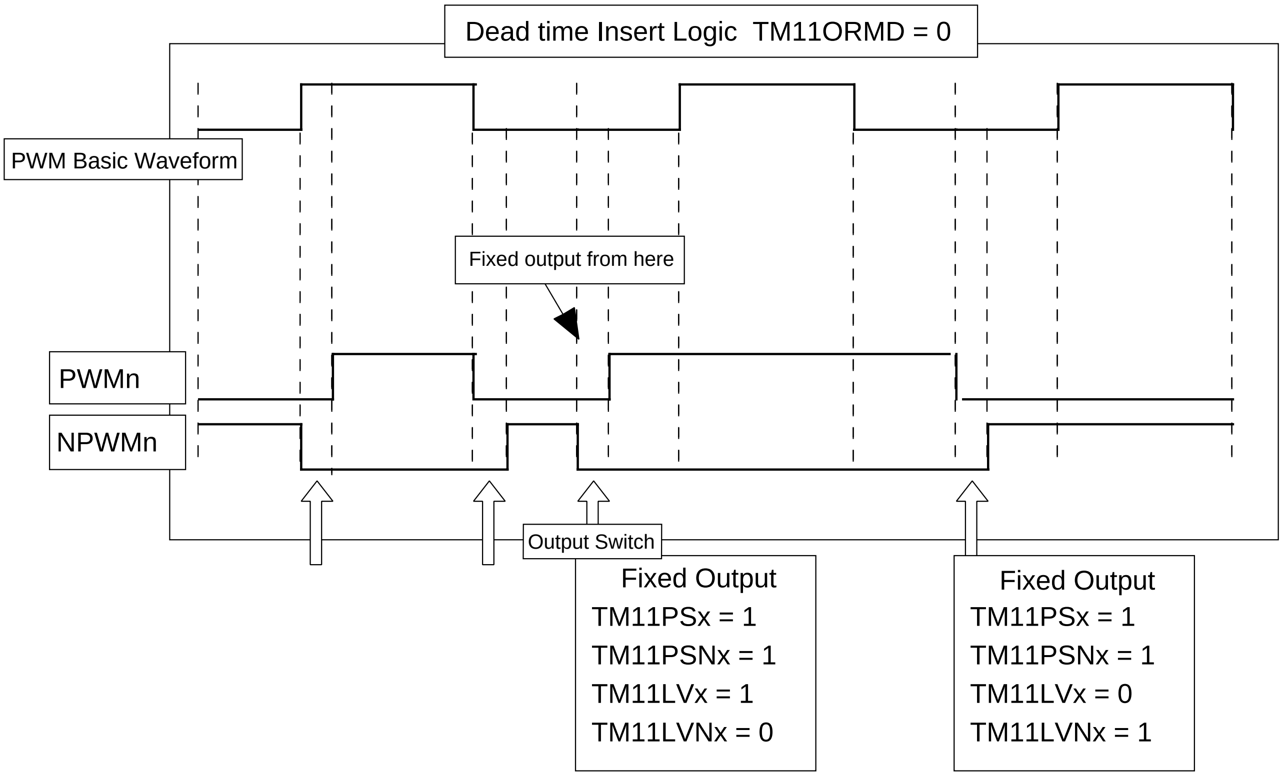
bp6 to 11 of Timer 11 output control register (TM11SL)
Switch of PWM output and fixed output can be set for each six PWM pins. The default value is ‘0’ for PWM output (1: fixed output, 0: PWM output).

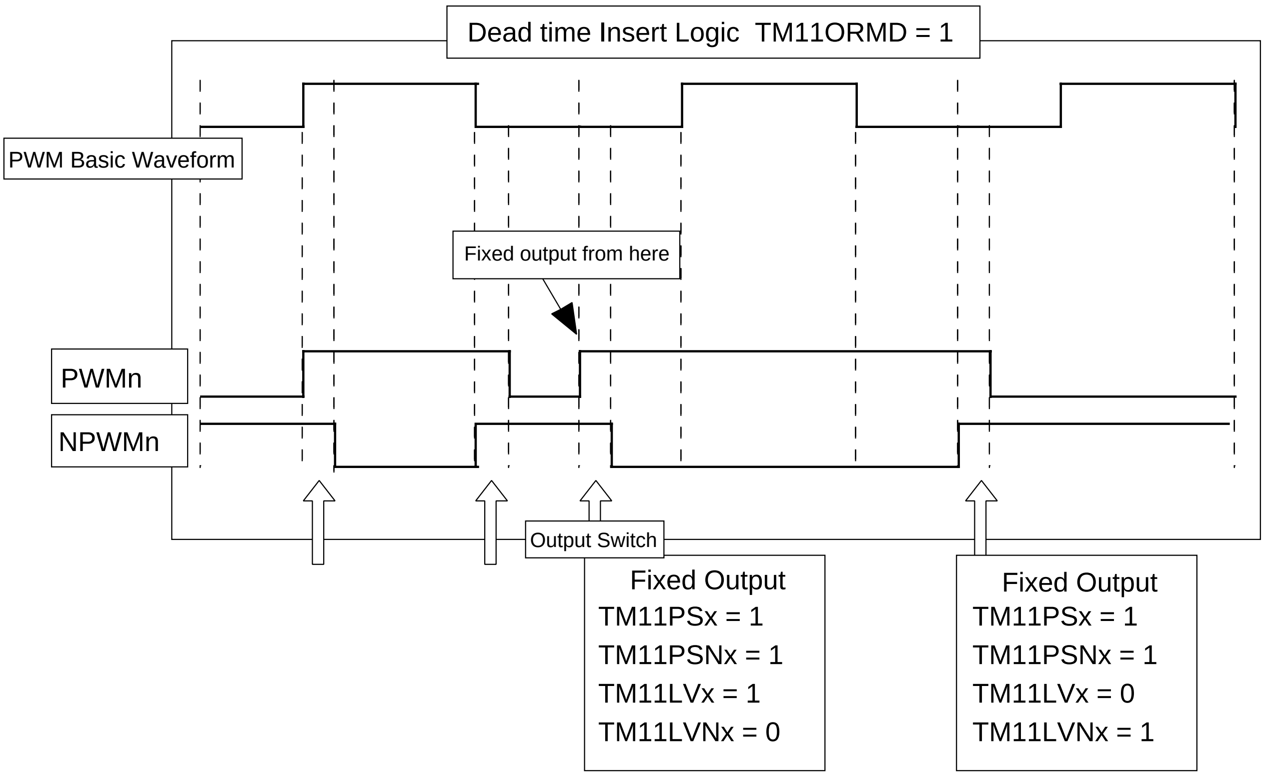
bp0 to 5 of Timer 11 output control register (TM11SL)
Select ‘H’ or ‘L’ to fix output. Selection can be set for each PWM pin. The default value is ‘0’ for ‘L’ fixing (1: ‘H’ fixing, 0: ‘L’ fixing).
TM11SL register has two choice: single buffer or double buffer. The output signal can be switched at the timing synchronized with Timer 11 counter value by setting register read timing of double buffer.



Dead time insert at fixed output

Dead time is inserted as delay at signal switching timing, so it is also inserted when PWM output is switched to fixed output.





4-5 Buzzer Output

4-5-1 Buzzer Output Setup and Operation

The square wave of system clock divided by $1/2^{12}$ to $1/2^{15}$ can be output to (P70, BUZZ).

(1) Set watchdog expansion and BZEN of buzzer output control register (WDREG) to '0' (Buzzer output is off.), and set buzzer output frequency by BZP1 and 0. For example here is $1/2^{12}$ dividing selected.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD CLR	—	—	—	—	—	WD P1	WD P0	—	—	—	—	—	BZEN	BZP1	BZP0
0						0	0						0	1	1

(2) Set BUZZ (P70) pin to output by the port 7 I/O control register (P7DIR) and the port 7 output mode register (P7MD).

P7DIR: x'00FFE7'

7	6	5	4	3	2	1	0
P7 DIR7	P7 DIR6	P7 DIR5	P7 DIR4	P7 DIR3	P7 DIR2	P7 DIR1	P7 DIR0
0	0	0	0	0	0	0	1

P7MD: x'00FFFC'

7	6	5	4	3	2	1	0
—	P7 MD6	—	—	—	—	—	P7 MD0
-	0	-	-	-	-	-	1

(3) Buzzer output status (ON or OFF) is controlled by BZEN flag of WDREG.

Chapter 5 Serial Interface

5-1 Overview

This LSI serial interface has 2 channels, and it is used for both communication types of clock synchronous and UART.

5-1-1 Functions

Table 5-1-1 shows functions of serial interface.

Table 5-1-1 Serial Interface Functions

Communication style	Clock synchronous	UART (half-duplex)
Channel	ch0, 1	ch0, 1
Interrupt	Transfer complete interrupt	Transfer complete interrupt
3 channels type	√	-
2 channels type	√ (SBO, SBT)	√
1 channel type	-	√ (TXD)
Specification of transfer bit count / flame selection	1 to 8 btis	7 bits + 1 STOP 7 bits + 2 STOPs 8 bits + 1 STOP 8 bits + 2 STOPs
Parity bit status	-	√
Parity bit control	-	0 parity 1 parity odd parity even parity
Selection of start condition	√	No selection Start bit is always added.
Specification of the first transfer bit	√	√
Specification of input edge / output edge	√	-
Continuous operation	√	√
Internal clock 1/8 dividing	√	Only 1/8 dividing is available.
Clock source	f_s/2 f_s/4 f_s/16 Timer 3 output/2 External clock	f_s/2 f_s/4 f_s/16 Timer 3 output/2
Maximum transfer rate	2.5 Mbps	300 kbps (Timer 3 output)
f_s: System clock When transmission and reception are operated at the same time at clock synchronous communication, select "no start condition".		

5-1-2 Block Diagram

■ Serial interface 0 Block Diagram

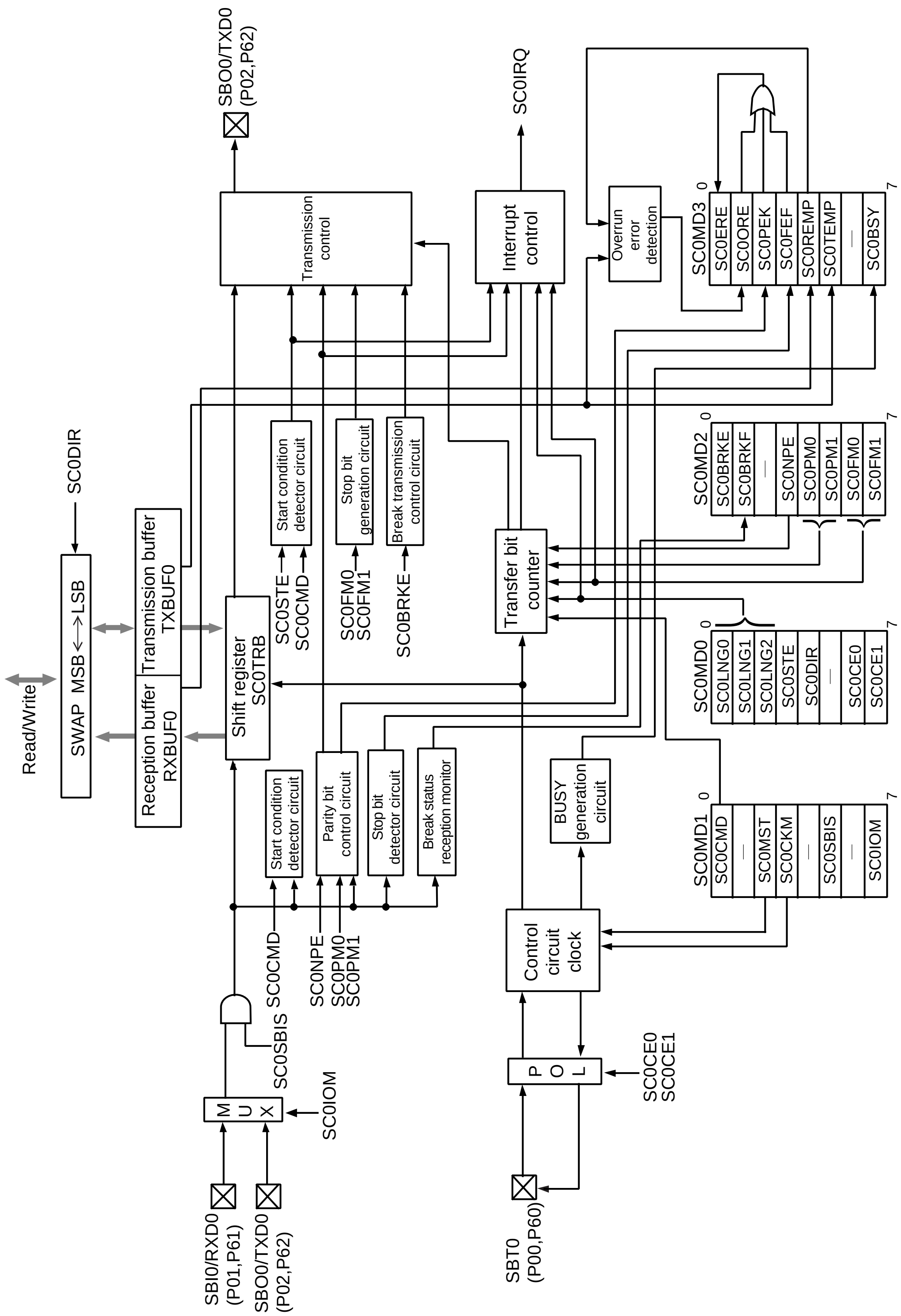


Figure 5-1-1 Serial Interface 0 Block Diagram

■ Serial interface 1 Block Diagram

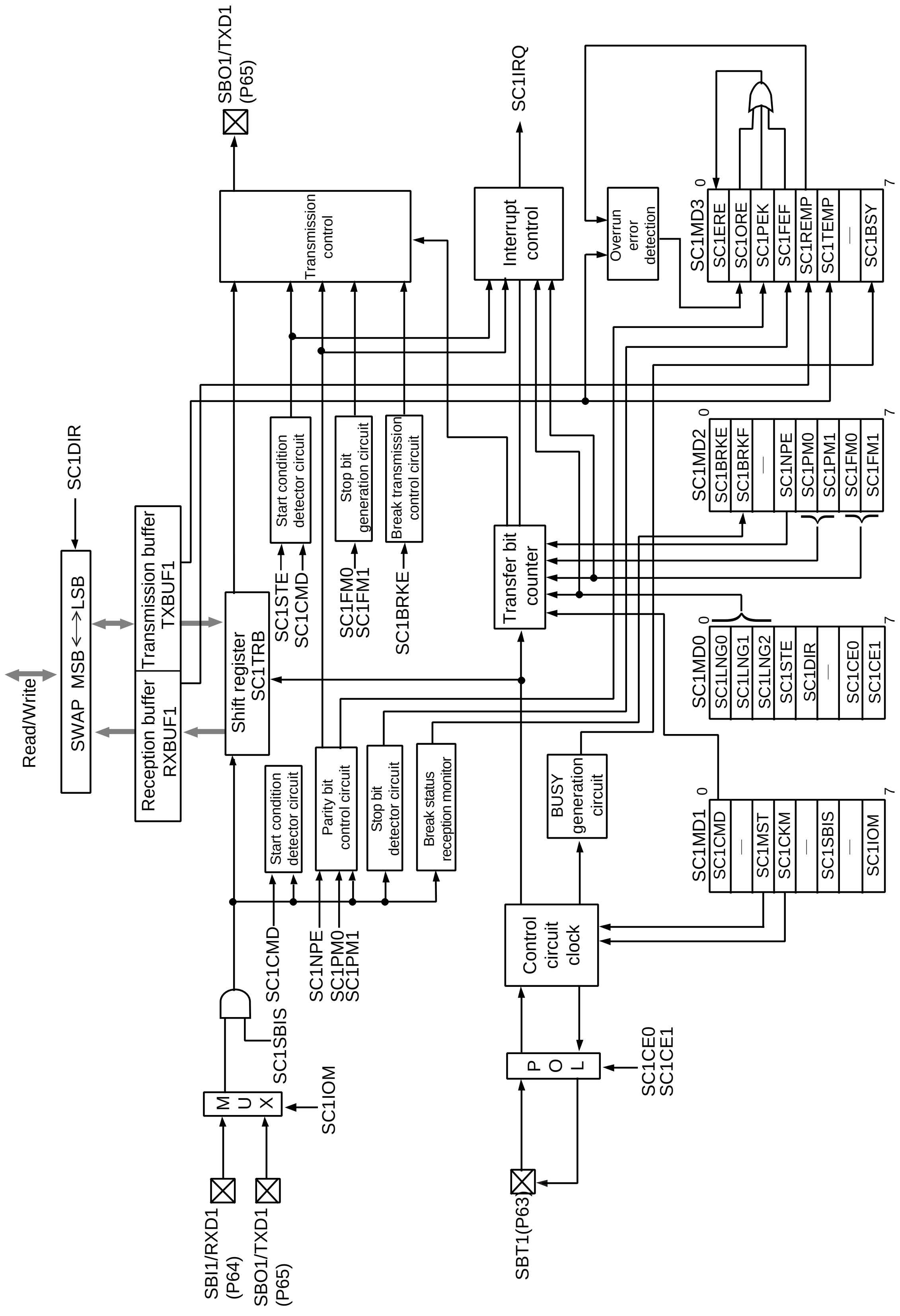


Figure 5-1-2 Serial Interface 1 Block Diagram

5-2 Control Registers

5-2-1 Registers

Table 5-2-1 shows registers to control serial interface.

[☞ Chapter 8   8-2-1 Special Function Registers]

Table 5-2-1 Serial Interface Control Registers

	Register	Address	R/W	Function
Serial interface 0	SC0MD0	X'00FD80'	R/W	Serial interface0 mode register 0
	SC0MD1	X'00FD81'	R/W	Serial interface0 mode register 1
	SC0MD2	X'00FD82'	R/W	Serial interface0 mode register 2
	SC0MD3	X'00FD83'	R	Serial interface0 mode register 3
	SC0CKS	X'00FD84'	R/W	Serial interface0 clock source control register
	RXBUF0	X'00FD86'	R	Serial interface0 reception buffer
	TXBUF0	X'00FD87'	R/W	Serial interface0 transmission buffer
Serial interface 1	SC1MD0	X'00FD90'	R/W	Serial interface1 mode register 0
	SC1MD1	X'00FD91'	R/W	Serial interface1 mode register 1
	SC1MD2	X'00FD92'	R/W	Serial interface1 mode register 2
	SC1MD3	X'00FD93'	R	Serial interface1 mode register 3
	SC1CKS	X'00FD94'	R/W	Serial interface1 clock source control register
	RXBUF1	X'00FD96'	R	Serial interface1 reception buffer
	TXBUF1	X'00FD97'	R/W	Serial interface1 transmission buffer

5-3 Operation

Serial interface can be used for both clock synchronous and half-duplex UART.

5-3-1 Clock Synchronous Serial Interface

■ Activation Factor for Communication

Table 5-3-1 shows activation factors for communication. At master communication, the transfer clock is generated by setting data to the transmission data buffer TXBUF0, or by receiving a start condition. Except for during communication, signal input from SBTO pin within serial interface is masked to prevent a malfunction by noise. This mask is automatically cancelled by setting data to TXBUF0 (This means to access TXBUF0 register.) or inputting a start condition to a data input pin. Therefore, at slave communication, input the external clock after setting data to TXBUF0 or inputting a start condition. Be sure to input the external clock after waiting for more than 2.5 transfer clock from setting data to TXBUF0. This waiting time is for loading data for internal shift register from TXBUF0. (These are the same for serial interface 1.)

Table 5-3-1 Synchronous Serial Interface Activation Factor

	Activation factor	
	Transmission	Reception
Master communication	Set reception data	Set dummy data
		Input start condition
Slave communication	Input clock after setting reception data	Input clock after setting dummy data
		Input clock after inputting start condition

■ Transfer Bit Count

The transfer bit count is selected from 1 bit to 8 bits. Set it by the SC0LNG2 to 0 flags of the SC0MD0 register (at reset: 111). Until resetting, SC0LNG2 to 0 flags maintain the previous setting value. (These are the same for serial interface 1.)

Except for during communication, SBT pin is masked within serial interface. At slave communication, be sure to input clock to SBT pin after setting data to TXBUF or inputting a start condition.

Before inputting external clock, wait for more than 2.5 transfer clock after setting data to TXBUF.

■ Start Condition

The SC0STE flag of the SC0MD0 register sets if a start condition is enabled or not. If a start condition is enabled and is input during communication, a bit counter is cleared to restart the communication. The start condition is regarded when a data line (SBI0 pin (with 3 channels) or SBO0 pin (with 2 channels)) changes from ‘H’ to ‘L’ with a clock line (SBT0 pin) being ‘H’. When the reception and the transmission should be operated at the same time, disable start condition for proper operation. (These are the same for serial interface 1.)

■ First Transfer Bit

The SC0DIR flag of the SC0MD0 register can set the first transfer bit. MSB first or LSB first can be selected. (These are the same for serial interface 1.)

■ Transmission Data Buffer

The transmission data buffer TXBUF0 is the sub-buffer to store data that is loaded in the internal shift register. Set the transmission data to the transmission data buffer TXBUF0. Data is automatically loaded in the internal shift register. The period for 2.5 transfer clock is needed to load data. During loading data, if data is reset to TXBUF0, it could not operate correctly. To confirm if data is being loaded or not, monitor the transmission buffer empty flag SC0TEMP of the SC0MD3. When data is set to TXBUF0, SC0TEMP flag is set to “1”, and after loading data it is automatically cleared to “0”. (These are the same for serial interface 1.)

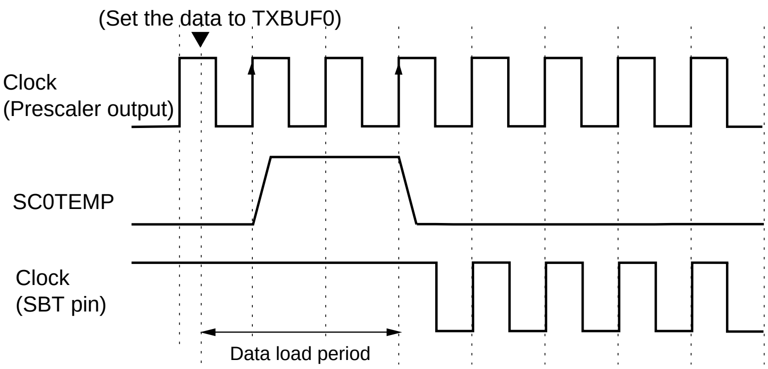


Figure 5-3-1 Data Load Period and the Transfer Buffer Empty Flag Operation

On the clock synchronous communication, if start condition is enable, the reception and transmission should not be operated at the same time. It can lead a malfunction.

If start condition is input and reset during transmission, the transmission data is invalid. If retransmission is needed, set the transmission data to TXBUF again.

RXBUF is overwritten every time transmission is over. For serial interface reception, read the data of RXBUF before next reception is completed.

■ Transfer Bit Count and First Transfer Bit

On transmission, when transfer bit is 1 bit to 7 bits, the data storing method to the transmission data buffer TXBUF0 is different depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUF0. When there are 6 bits to be transmitted, as shown on figure 5-3-2-1, if data “A” to “F” are stored to bp2 to bp7 of TXBUF0, the transmission is started from “F” to “A”. At LSB first, use the lower bits of TXBUF0. When there are 6 bits to be transmitted, as shown on figure 5-3-2-2, if data “A” to “F” are stored to bp5 to bp0 of TXBUF0, the transmission is started from “A” to “F”. (These are the same for serial interface 1.)

	7	6	5	4	3	2	1	0
TXBUF	F	E	D	C	B	A		

Figure 5-3-2-1 Transfer Bit Count and First Transfer Bit (Starting with MSB)

	7	6	5	4	3	2	1	0
TXBUF			F	E	D	C	B	A

Figure 5-3-2-2 Transfer Bit Count and First Transfer Bit (Starting with LSB)

■ Received Data Buffer

The reception data buffer RXBUF0 is the sub-buffer that pushes the reception data in the internal shift register. After the communication complete interrupt SC0IRQ is generated, the data (regardless transmission or reception) stored in the internal shift register is automatically stored in the reception data buffer RXBUF0. RXBUF0 can store data up to 1 byte. RXBUF0 is overwritten every time transmission is over, so read the data of RXBUF0 before the next reception is completed. Only when SC0SBIS flag of SC0MD1 register is set to “serial interface input”, the reception buffer empty flag SC0REMP is set to “1” at the same time when SC0IRQ is generated. SC0REMP is cleared to “0” after reading RXBUF0. (These are the same for serial interface 1.)

■ Received Bit Count and First Transfer Bit

On reception, when transfer bit is 1 bit to 7 bits, the data storing method to the reception data buffer RXBUF0 is different depending on the first transfer bit selection. At MSB first, data is stored in the lower bits of RXBUF0. When there are 6 bits to be transmitted, as shown on figure 5-3-3-1, data “A” to “F” are stored to bp0 to bp5 of RXBUF0 from “F” to “A”. At LSB first, data is stored to the upper bits of RXBUF0. When there are 6 transfer bits to be transmitted, as shown on figure 5-3-3-2, data “A” to “F” are stored to bp2 to bp7 of RXBUF0 from “A” to “F”. (These are the same for serial interface 1.)

	7	6	5	4	3	2	1	0
RXBUF			F	E	D	C	B	A

Figure 5-3-3-1 Reception Bit Count and First Transfer Bit (Starting with MSB)

	7	6	5	4	3	2	1	0
RXBUF	F	E	D	C	B	A		

Figure 5-3-3-2 Reception Bit Count and First Transfer Bit (Starting with LSB)

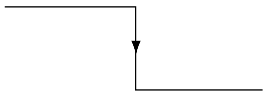
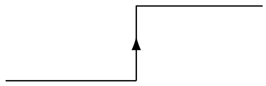
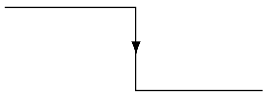
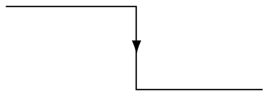
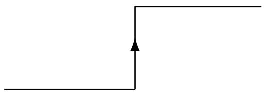
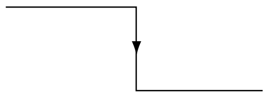
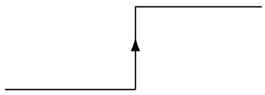
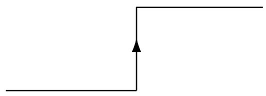
■ Contiguous communication

This serial interface has continued transmission function. During communication, if data is set to the transmission data buffer TXBUF0, the transmission buffer empty flag SC0TEMP is set, and automatically and continuously transmitted. Set data to TXBUF0 between loading data to the internal shift register and generating the communication complete interrupt SC0IRQ. At master communication, the communication blank from generating SC0IRQ to the next transfer clock output is 3 transfer cycles. (These are the same for serial interface 1.)

■ Input Edge/Output Edge Setup

SC0CE1 to 0 flags of SC0MD0 register set an output edge of the transmission data and an input edge of the reception data. As the SC0CE1 flag = ”0”, the transmission data is output at the falling edge, and as “1”, output at the rising edge. As SC0CE0 =”0”, the reception data is stored at the inversion edge to the output edge of the transmission data, and as “1”, stored at the same edge with the output edge of the transmission data. (These are the same for serial interface 1.)

Table 5-3-2 Input Edge and Output Edge of Transmission/Reception Data

SC0CE1	SC0CE0	Transmission data output edge	Reception data input edge
0	0		
0	1		
1	0		
1	1		

■ Clock Setup

Clock source is selected by the SC0CKS register (X'00FD84'). The internal clock (clock master) or external clock (clock slave) can be selected by the SC0MST flag of the SC0MD1 register. Even when the external clock is selected, set the internal clock whose clock cycle is not more than the external clock by the SC0CKS register. This is because the internal clock generates the interrupt flag SC0IRQ. Table 5-3-3 shows internal clock source set by the SC0CKS register. The SC0CKM flag of the SC0MD1 register can divide the internal clock by eight in addition. (These are the same for serial interface 1.)

Table 5-3-3 Synchronous Serial Interface internal Clock Source

	Serial interface 0 and 1
Clock source (Internal clock)	fs/2
	fs/4
	fs/16
	Timer 3 output/2

■ Data Input Pin Setup

3 channels type (clock pin (SBT0 pin), data output pin (SBO0 pin) and data input pin (SBI0 pin)) or 2 channels type (clock pin (SBT0 pin) and data I/O pin (SBO0 pin)) can be selected as the communication. SBI0 pin can be used only for serial data input. SBO0 pin can be used for serial data input or output. The SC0IOM flag of the SC0MD1 register can select if the serial data is input from SBI0 pin or SBO0 pin. When "data input from SBO0 pin" is selected to set the 2 channels type, transmission and reception can be switched by controlling the direction of SBO0 pin with I/O control register of port0 and port6, and output mode register. At that time, SBI0 pin is free to be used as a general port. Refer to Chapter 7 Port Function for detail. (These are the same for serial interface 1.)

The maximum transfer rate is 2.5 MHz. When transfer clock is more than 2.5 MHz, the transmission data can not be delivered normally.

At reception, if SC0IOM of the SC0MD1 register is set to "1" and "serial data input from SBO pin" is selected, SBI pin can be used as a general port.

■ Reception Buffer Empty Flag

When communication complete interrupt SC0IRQ is generated, data is automatically stored from the internal shift register to RXBUF0. If data is stored to the shift register RXBUF0 with the SC0SBIS flag of the SC0MD1 register set to “serial interface input”, the reception buffer empty flag SC0REMP of the SC0MD3 register is set to “1”. This means the reception data is waiting to be read. SC0REMP is cleared to “0” by reading data of RXBUF0. (These are the same for serial interface 1.)

■ Transmission Buffer Empty Flag

When data is set to TXBUF0 during communication (between loading data to the internal shift register and generating communication complete interrupt SC0IRQ), the transmission buffer empty flag SC0TEMP of SC0MD3 is set to “1”. This means the next transmission data is waiting to be loaded. Data is loaded from TXBUF0 to the internal shift register by generating SC0IRQ. At the same time when SC0TEMP is cleared to “0”, the next communication is automatically started. (These are the same for serial interface 1.)

■ Overrun Error and Error Monitor Flag

After reception is completed, if the next data reception is completed before data of the reception data buffer RXBUF0 starts to be read, overrun error occurs and the SC0ORE flag of SC0MD3 is set to “1”. At the same time, the error monitor flag SC0ERE is set, it shows error occurred at reception. The SC0ORE flag stays the same unless the data of RXBUF0 is read. SC0ERE is cleared at the same time when SC0ORE is cleared. These error flags do not have influence to communication operation. (These are the same for serial interface 1.)

■ BUSY flag

When data is set to TXBUF0 or start condition is recognized, the BUSY flag SC0BSY of the SC0MD3 register is set to “1”. When communication complete interrupt SC0IRQ is generated, it is cleared to “0”. During contiguous communication, SC0BSY stays the same. When communication complete interrupt SC0IRQ is generated, if the transmission buffer empty flag SC0TEMP is cleared to “0”, SC0BSY flag is cleared to “0”. (These are the same for serial interface 1.)

■ Last bit of transfer data

Table 5-3-4 shows data output maintain period of last bit at transmission and minimum data input period of last bit at reception. The internal clock has to be set at slave. This keeps data hold time at data transmission. After data output maintain period of last bit, “H” is output.

Table 5-3-4 Last Bit Data Length of Transfer Data

	At transmission Last bit data maintain period	At reception Last bit data input period
At master	1 bit data length	1 bit data length (minimum)
At slave	[1 bit data length of external clock × 1/2] + [Internal clock cycle × 1/2 to 1)]	

■ Other Control Flags

Flags shown in table 5-3-5 are not used for clock synchronous communication, so they are not needed to be set or monitored. (This is the same for serial interface 1.)

Table 5-3-5 Other Control Flags

Register	Flag	Detail
SC0MD2	SC0BRKF	Break status reception monitor
	SC0NPE	Parity is enable.
	SC0PM1 to 0	Added bit specification
	SC0FM1 to 0	Frame mode specification
SC0MD3	SC0PEK	Parity error detection
	SC0FEF	Frame error detection

■ Transmission Timing

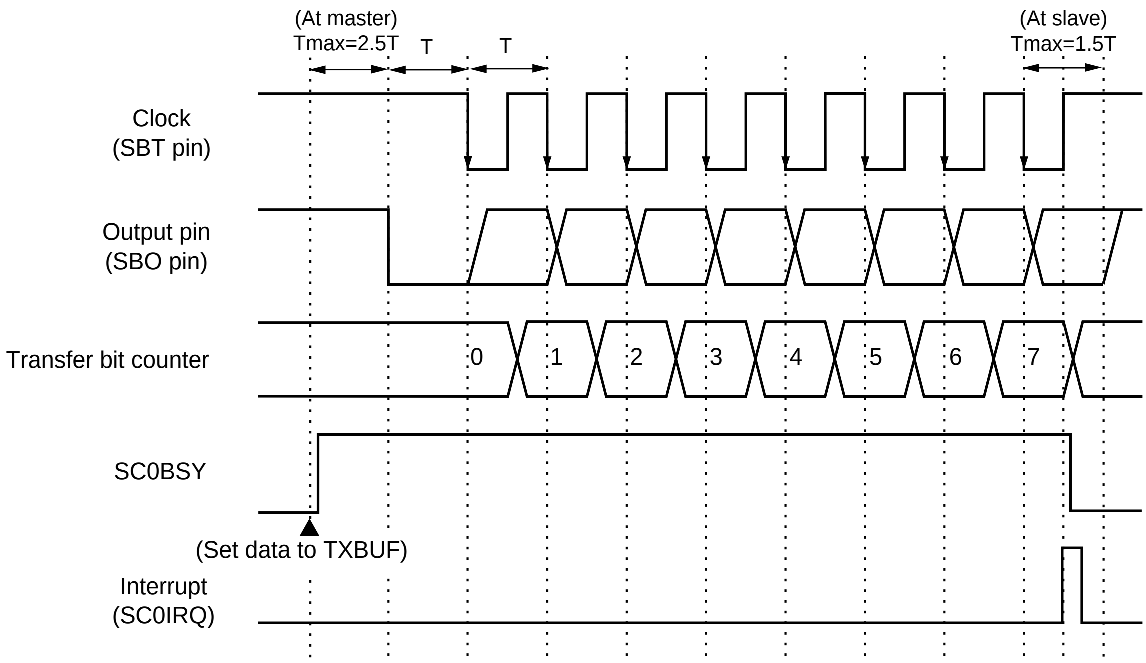


Figure 5-3-4 Transmission Timing (Falling Edge, Start Condition Enabled)

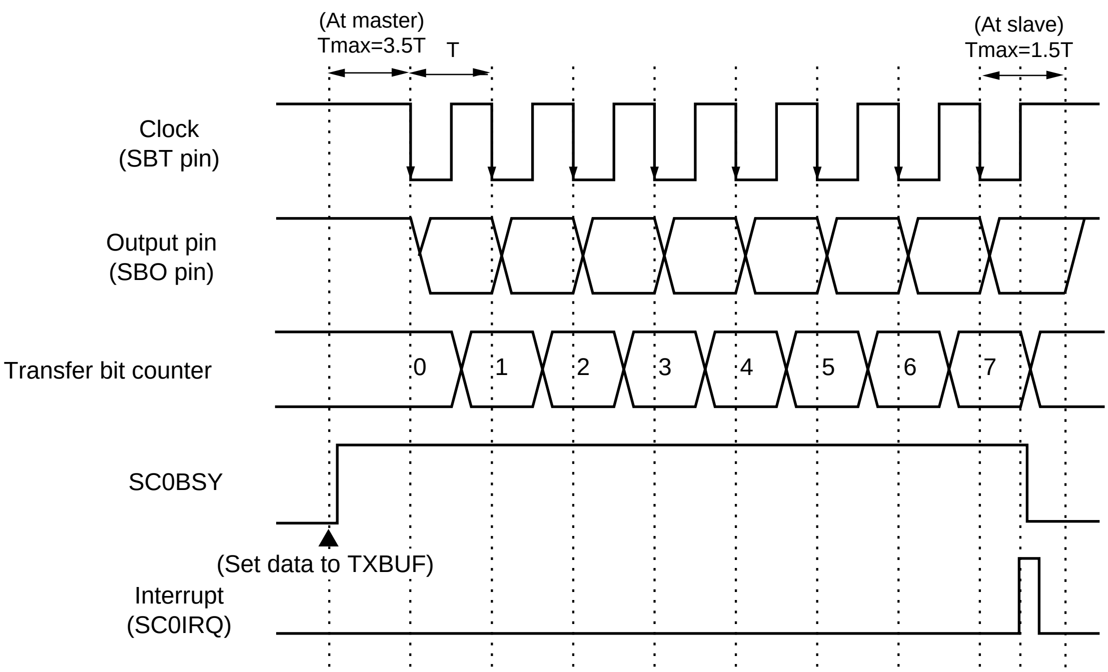


Figure 5-3-5 Transmission Timing (Falling Edge, Start Condition Disabled)

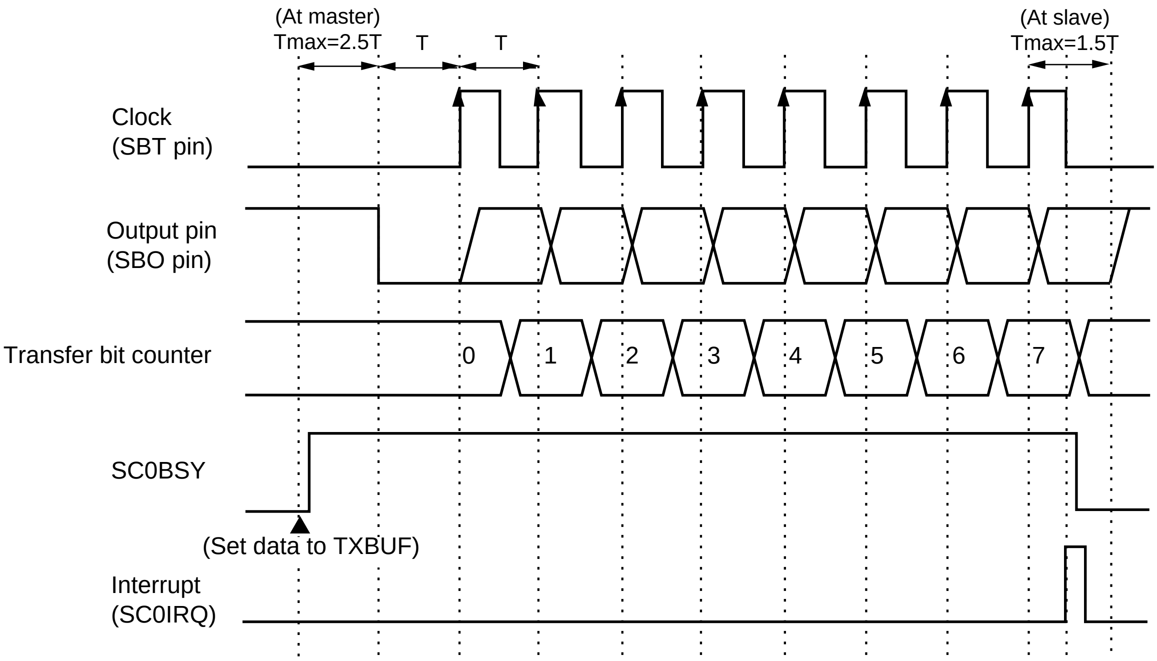


Figure 5-3-6 Transmission Timing (Rising Edge, Start Condition Enabled)

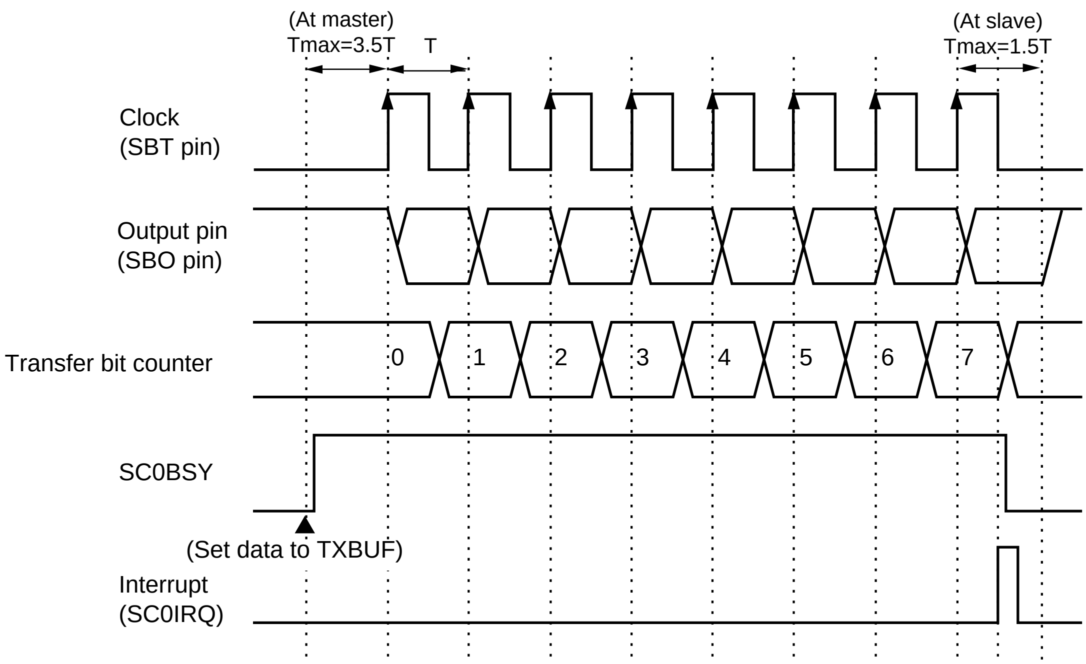


Figure 5-3-7 Transmission Timing (Rising Edge, Start Condition Disabled)

■ Reception Timing

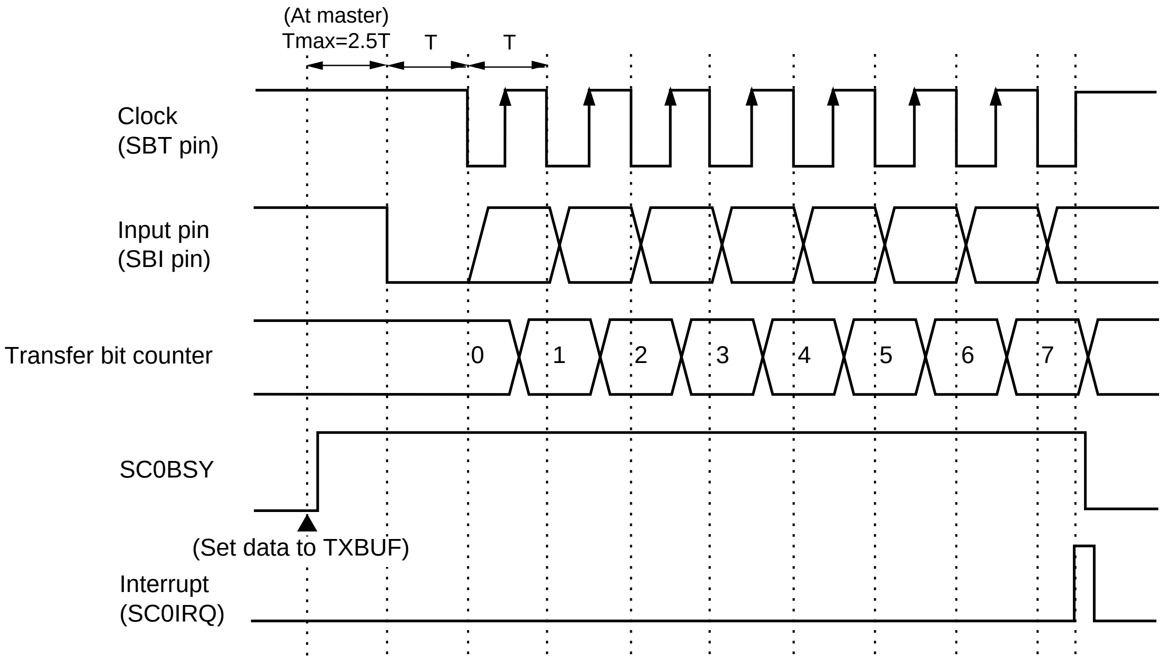


Figure 5-3-8 Reception Timing (Rising Edge, Start Condition Enabled)

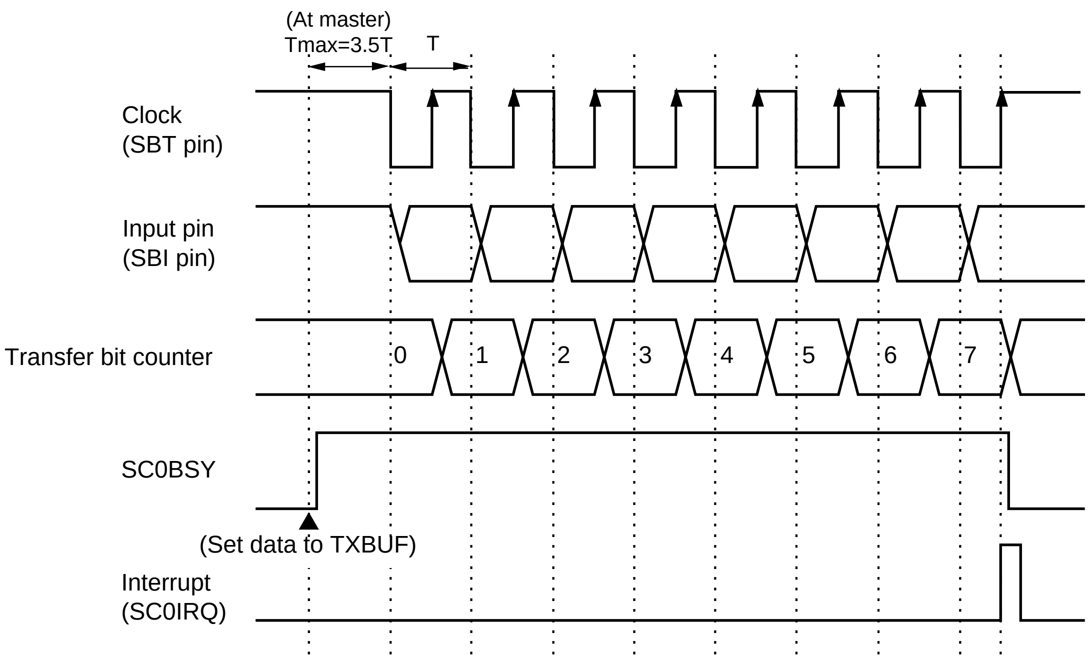


Figure 5-3-9 Reception Timing (Rising Edge, Start Condition Disabled)

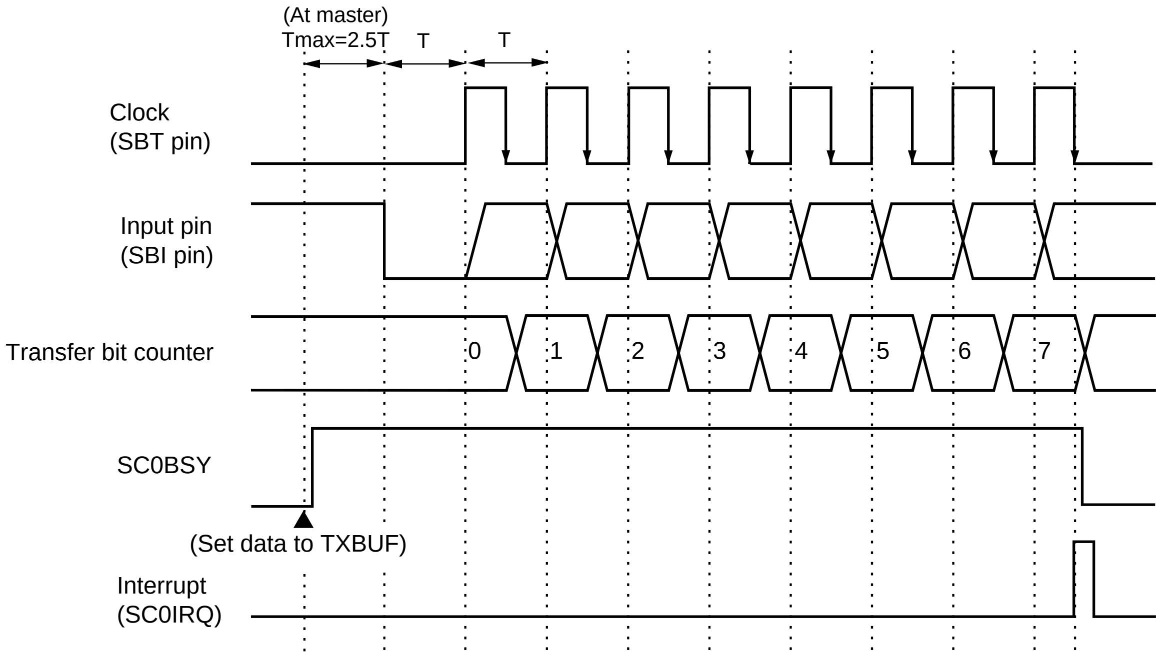


Figure 5-3-10 Reception Timing (Falling Edge, Start Condition Enabled)

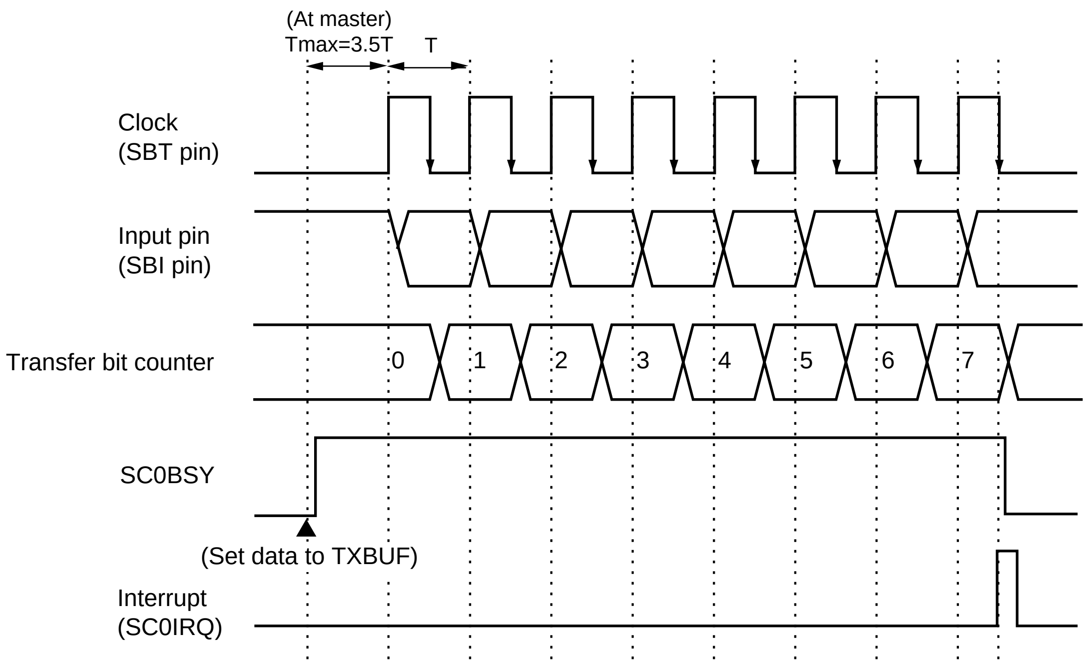


Figure 5-3-11 Reception Timing (Falling Edge, Start Condition Disabled)

■ Transmission / Reception Simultaneous Timing

When transmission and reception are operated at the same time, set the SC0CE1 to 0 flags of the SC0MD0 register to “00” or “10”. Data is received at the opposite edge timing of the transmission clock, so that the reception clock should be the opposite edge of the transmission clock from the other side.
(These are the same for serial interface 1.)

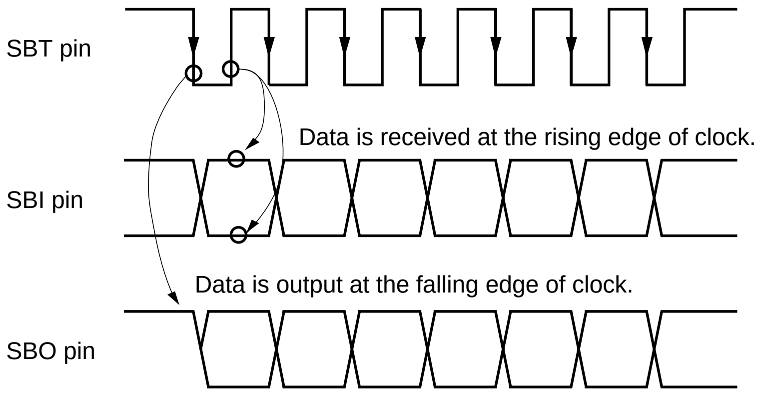


Figure 5-3-12 Transmission / Reception Timing
(Reception: Rising Edge, Transmission: Falling Edge)

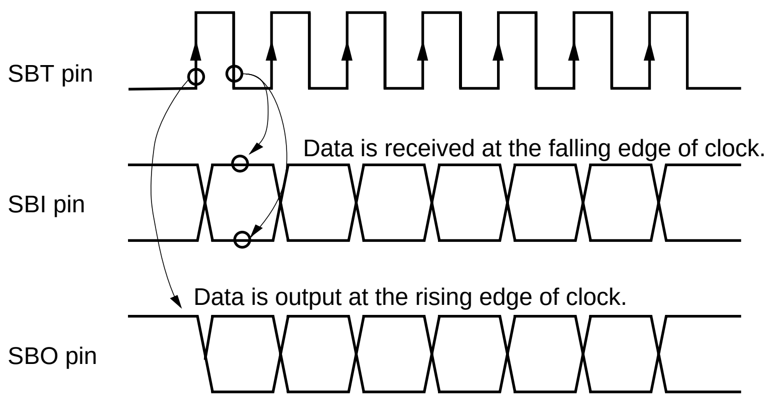


Figure 5-3-13 Transmission / Reception Timing
(Reception: Falling Edge, Transmission: Rising Edge)

■ Pins Setup (3 Channels, at Transmission)

Table 5-3-6 shows the setup for synchronous serial interface pins with 3 channels (SBO pin, SBI pin and SBT pin) at transmission.

Table 5-3-6 Setup for Synchronous Serial Interface Pins (3 Channels, at Transmission)

<table>
<tr><td rowspan="3">Setup item</td><td>Data output pin</td><td>Data input pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO pin</td><td rowspan="2">SBI pin</td><td colspan="2">SBT pin</td></tr>
<tr><td>Internal clock</td><td>External clock</td></tr>
<tr><td colspan="5">Serial interface 0</td></tr>
<tr><td>Pin</td><td>P02 (P62)</td><td>P01 (P61)</td><td colspan="2">P00 (P60)</td></tr>
<tr><td rowspan="2">SBI/SBO pin</td><td colspan="2">SBI0/SBO0 independent</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC0MD1 (SC0IOM)</td></tr>
<tr><td rowspan="2">SBI input control</td><td rowspan="2">-</td><td>Input "1"</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td>SC0MD1 (SC0SBIS)</td></tr>
<tr><td rowspan="2">SBT clock</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Master</td><td>Slave</td></tr>
<tr><td colspan="2">SC0MD1 (SC0MST)</td></tr>
<tr><td rowspan="2">Style</td><td>Push-pull/
Nch open-drain</td><td rowspan="2">-</td><td>Push-pull/
Nch open-drain</td><td>Push-pull/
Nch open-drain</td></tr>
<tr><td>SC0CKS (SC0ODC1)</td><td colspan="2">SC0CKS (SC0ODC0)</td></tr>
<tr><td>Port</td><td colspan="4">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
<tr><td colspan="5">Serial interface 1</td></tr>
<tr><td>Pin</td><td>P65</td><td>P64</td><td colspan="2">P63</td></tr>
<tr><td rowspan="2">SBI/SBO pin</td><td colspan="2">SBI1/SBO1 independent</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC1MD1 (SC1IOM)</td></tr>
<tr><td rowspan="2">SBI input control</td><td rowspan="2">-</td><td>Input "1"</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td>SC1MD1 (SC1SBIS)</td></tr>
<tr><td rowspan="2">SBT clock</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Master</td><td>Slave</td></tr>
<tr><td colspan="2">SC1MD1 (SC0MST)</td></tr>
<tr><td rowspan="2">Style</td><td>Push-pull/
Nch open-drain</td><td rowspan="2">-</td><td>Push-pull/
Nch open-drain</td><td>Push-pull/
Nch open-drain</td></tr>
<tr><td>SC1CKS (SC1ODC1)</td><td colspan="2">SC1CKS (SC1ODC0)</td></tr>
<tr><td>Port</td><td colspan="4">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
</table>

■ Pins Setup (3 Channels, at Reception)

Table 5-3-7 shows the setup for synchronous serial interface pins with 3 channels (SBO pin, SBI pin and SBT pin) at reception.

Table 5-3-7 Setup for Synchronous Serial Interface Pins (3 Channels, at Reception)

<table>
<tr><td rowspan="3">Setup item</td><td>Data output pin</td><td>Data input pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO pin</td><td rowspan="2">SBI pin</td><td colspan="2">SBT pin</td></tr>
<tr><td>Internal clock</td><td>External clock</td></tr>
<tr><td colspan="5">Serial interface 0</td></tr>
<tr><td>Pin</td><td>P02 (P62)</td><td>P01 (P61)</td><td colspan="2">P00 (P60)</td></tr>
<tr><td rowspan="2">SBI/SBO pin</td><td colspan="2">SBI0/SBO0 independent</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC0MD1 (SC0IOM)</td></tr>
<tr><td rowspan="2">SBI input control</td><td rowspan="2">-</td><td>Serial data input</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td>SC0MD1 (SC0SBIS)</td></tr>
<tr><td rowspan="2">SBT clock</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Master</td><td>Slave</td></tr>
<tr><td colspan="2">SC0MD1 (SC0MST)</td></tr>
<tr><td rowspan="2">Style</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Push-pull/
Nch open-drain</td><td>Push-pull/
Nch open-drain</td></tr>
<tr><td colspan="2">SC0CKS (SC0ODC0)</td></tr>
<tr><td>Port</td><td colspan="4">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
<tr><td colspan="5">Serial interface 1</td></tr>
<tr><td>Pin</td><td>P65</td><td>P64</td><td colspan="2">P63</td></tr>
<tr><td rowspan="2">SBI/SBO pin</td><td colspan="2">SBI1/SBO1 independent</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC1MD1 (SC1IOM)</td></tr>
<tr><td rowspan="2">SBI input control</td><td rowspan="2">-</td><td>Serial data input</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td>SC1MD1 (SC1SBIS)</td></tr>
<tr><td rowspan="2">SBT clock</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Master</td><td>Slave</td></tr>
<tr><td colspan="2">SC1MD1 (SC0MST)</td></tr>
<tr><td rowspan="2">Style</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Push-pull/
Nch open-drain</td><td>Push-pull/
Nch open-drain</td></tr>
<tr><td colspan="2">SC1CKS (SC1ODC0)</td></tr>
<tr><td>Port</td><td colspan="4">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
</table>

■ Pins Setup (3 Channels, at Transmission/Reception)

Table 5-3-8 shows the setup for synchronous serial interface pins with 3 channels (SBO pin, SBI pin and SBT pin) at transmission/reception.

Table 5-3-8 Setup for Synchronous Serial Interface Pins (3 Channels, at Transmission/Reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO pin	SBI pin	SBT pin	
			Internal clock	External clock
Serial interface 0				
Pin	P02 (P62)	P01 (P61)	P00 (P60)	
SBI/SBO pin	SBI0/SBO0 independent		-	
	SC0MD1 (SC0IOM)			
SBI input control	-	Serial data input	-	
		SC0MD1 (SC0SBIS)		
SBT clock	-	-	Master	Slave
			SC0MD1 (SC0MST)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	SC0CKS (SC0ODC1)		SC0CKS (SC0ODC0)	
Port	Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.			
Serial interface 1				
Pin	P65	P64	P63	
SBI/SBO pin	SBI1/SBO1 independent		-	
	SC1MD1 (SC1IOM)			
SBI input control	-	Serial data input	-	
		SC1MD1 (SC1SBIS)		
SBT clock	-	-	Master	Slave
			SC1MD1 (SC0MST)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	SC1CKS (SC1ODC1)		SC1CKS (SC1ODC0)	
Port	Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.			

■ Pins Setup (2 Channels, at Transmission)

Table 5-3-9 shows the setup for synchronous serial interface pins with 2 channels (SBO pin and SBI pin) at transmission. SBI pin is free to be used as a general port.

Table 5-3-9 Setup for Synchronous Serial Interface Pins (2 Channels, at Transmission)

<table>
<tr><td rowspan="3">Setup item</td><td>Data outptu pin</td><td>Serial unused pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO pin</td><td rowspan="2">SBI pin</td><td colspan="2">SBT pin</td></tr>
<tr><td>Internal clock</td><td>External clock</td></tr>
<tr><td colspan="5">Serial interface 0</td></tr>
<tr><td>Pin</td><td>P02 (P62)</td><td>P01 (P61)</td><td colspan="2">P00 (P60)</td></tr>
<tr><td rowspan="2">SBI/SBO pin</td><td colspan="2">SBI0/SBO0 connected</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC0MD1 (SC0IOM)</td></tr>
<tr><td rowspan="2">SBI input control</td><td rowspan="2">-</td><td>Input "1"</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td>SC0MD1 (SC0SBIS)</td></tr>
<tr><td rowspan="2">SBT clock</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Master</td><td>Slave</td></tr>
<tr><td colspan="2">SC0MD1 (SC0MST)</td></tr>
<tr><td rowspan="2">Style</td><td>Push-pull/ Nch open-drain</td><td rowspan="2">-</td><td>Push-pull/ Nch open-drain</td><td>Push-pull/ Nch open-drain</td></tr>
<tr><td>SC0CKS (SC0ODC1)</td><td colspan="2">SC0CKS (SC0ODC0)</td></tr>
<tr><td>Port</td><td colspan="4">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
<tr><td colspan="5">Serial interface1</td></tr>
<tr><td>Pin</td><td>P65</td><td>P64</td><td colspan="2">P63</td></tr>
<tr><td rowspan="2">SBI/SBO pin</td><td colspan="2">SBI1/SBO1 connected</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC1MD1 (SC1IOM)</td></tr>
<tr><td rowspan="2">SBI input control</td><td rowspan="2">-</td><td>Input "1"</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td>SC1MD1 (SC1SBIS)</td></tr>
<tr><td rowspan="2">SBT clock</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Master</td><td>Slave</td></tr>
<tr><td colspan="2">SC1MD1 (SC0MST)</td></tr>
<tr><td rowspan="2">Style</td><td>Push-pull/ Nch open-drain</td><td rowspan="2">-</td><td>Push-pull/ Nch open-drain</td><td>Push-pull/ Nch open-drain</td></tr>
<tr><td>SC1CKS (SC1ODC1)</td><td colspan="2">SC1CKS (SC1ODC0)</td></tr>
<tr><td>Port</td><td colspan="4">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
</table>

■ Pins Setup (2 Channels, at Reception)

Table 5-3-10 shows the setup for synchronous serial interface pins with 2 channels (SBO pin and SBI pin) at reception. SBI pin is free to be used as a general port.

Table 5-3-10 Setup for Synchronous Serial Interface Pins (2 Channels, at Reception)

Setup item	Data output pin	Serial unused pin	Clock I/O pin	
	SBO pin	SBI pin	SBT pin	
			Internal clock	External clock
Serial interface 0				
Pin	P02 (P62)	P01 (P61)	P00 (P60)	
SBI/SBO pin	SBI0/SBO0 connected		-	
	SC0MD1 (SC0IOM)			
SBI input control	-	Seral data input	-	
		SC0MD1 (SC0SBIS)		
SBT clock	-	-	Master	Slave
			SC0MD1 (SC0MST)	
Style	-	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
			SC0CKS (SC0ODC0)	
Port	Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.			
Serial interface 1				
Pin	P65	P64	P63	
SBI/SBO pin	SBI1/SBO1 connected		-	
	SC1MD1 (SC1IOM)			
SBI input control	-	Serial data input	-	
		SC1MD1 (SC1SBIS)		
SBT clock	-	-	Master	Slave
			SC1MD1 (SC0MST)	
Style	-	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
			SC1CKS (SC1ODC0)	
Port	Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.			

5-3-2 Setup Example

■ Transmission/Reception Setup Example

The setup example for clock synchronous serial interface communication with serial interface 0 is shown. Table 5-3-11 shows the conditions at transmission/reception.

Table 5-3-11 Setup Example for Synchronous Serial Interface Transmission/Reception

Setup item	Set to	Setup item	Set to
SBI0/SBO0 pin	Independent (with 3 channels)	Clock source	fs/2
Transfer bit count	8 bit	Clock source 1/8 dividing	Not divided by 8
Start condition	None	SBT1/SBO1 pin style	Nch open-drain
First transfer bit	MSB	Serila pin pull-up resistor	Added
Input clock edge	Falling edge		
Output clock edge	Rising edge	Serial 0 communication complete interrupt	Enable
Clock	Internal clock	Ports used for serial 0	P02 to P00

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set pins. P0MD (x'00FFF0') bp3, 0 : P0MD3, 0 = 1, 1 P0DIR (x'00FFE0') bp2-0 : P0DIR2-0 = 101 PMSEL (x'00FFA0') bp2-0 : PMSEL2-0 = 000	(1) With the P0MD register, the P0DIR register and the PMSEL register, set P02 to the serial data output pin SBO0, P01 to the serial data input pin SBI0 and P00 to the serial interface clock output pin SBT0.
(2) Set the interrupt. G3ICR (x'00FC46') bp14-12 : G3LV2-0 = 100 bp10 : SC0IE = 1 bp6 : SC0IR = 0 (bp15-0 = x'4400')	(2) Enable the interrupt. At this time, erase all former interrupt requests. That is set interrupt level (6 to 0) to G3LV2-0 of the maskable interrupt control register (group) 3 (G3ICR), and also set '1' to SC0IE and '0' to SC0IR. For example, write x'4400' to G3ICR. After this, when transmission of serial interface 0 is completed, the interrupt is occurred.
(3) Select the clock source. SC0CKS (x'00FD84') bp1-0 : SC0CS1-0 = 00	(3) Set the SC0CS1-0 flags of the SC0CKS register to "00" and select fs/2 for the clock source.

Setup Procedure	Description
(4) Control the pin type. SC0CKS (x'00FD84') bp3-2 : SC0ODC1-0 = 11 PPUPA (x'00FFB0') bp7 : PPUPA7 = 1	(4) Set the SC0ODC1-0 flags of the SC0CKS register to “11" to select Nch open-drain for SBO0/SBT0 pin type. Set the PPUPA7 flag of the PPUPA register to “1” to select “add pull-up resistor” for serial interface pin.
(5) Select the transfer bit count. SC0MD0 (x'00FD80') bp2-0 : SC0LNG2-0 = 111	(5) Set the SC0LNG2-0 of the serial interface 0 mode register (SC0MD0) to “111” to set the transfer bit count to 8 bits.
(6) Select the start condition. SC0MD0 (x'00FD80') bp3 : SC0STE = 0	(6) Set the SC0STE flag of the SC0MD0 register to “0” to disable start condition.
(7) Select the first bit to be transferred. SC0MD0 (x'00FD80') bp4 : SC0DIR = 0	(7) Set the SC0DIR flag of the SC0MD0 register to “0” to select MSB as a transfer first bit.
(8) Select the transfer edge. SC0MD0 (x'00FD80') bp6 : SC0CE0 = 0 bp7 : SC0CE1 = 1	(8) Set the SC0CE1, 0 flags of the SC0MD0 register to “1, 0 “ to set the transmission data output edge to “rising”, and the reception data input edge to “falling”.
(9) Control the output data. SC0MD2 (x'00FD82') bp0 : SC0BRKE = 0	(9) Set the SC0BRKE flag of the SC0MD2 register to “0” to select serial data transmission.
(10) Set other mode register. SC0MD2 (x'00FD82') bp7-3	(10) This is the setting flag for UART communication, not needed to be set for synchronous serial interface communication.
(11) Select the communication type. SC0MD1 (x'00FD81') bp0 : SC0CMD = 0	(11) Set the SC0CMD flag of the SC0MD1 register to “0” to select synchronous serial interface.
(12) Select the transfer clock. SC0MD1 (x'00FD81') bp2 : SC0MST = 1 bp3 : SC0CKM = 0	(12) Set the SC0MST flag of the SC0MD1 register to “1” to select clock master (internal clock). Set the SC0CKM flag to “1” not to divide clock source by 8.

Setup Procedure	Description
(13) Control the pin function. SC0MD1 (x'00FD81') bp5 : SC0SBIS = 1 bp7 : SC0IOM = 0	(13) Set the SC0SBIS flag of the SC0MD1 register to “1” to set SBI0 pin to “serial data input” by setting SC0IOM flag to “0”.
(14) Start the serial interface transmission. Transmitted data → TXBUF0(x’00FD87’) Received data → input it to SBI0 pin	(14) Set the transmission data to the serial interface transmission data buffer TXBUF0. The internal clock is generated to start transmission and reception. After transmission is completed, serial interface 0 transfer complete interrupt SC0IRQ is generated.

Note: (5) to (8) can be set at the same time, so can (9) and (10), and (11) to (13).

When only reception with 3 channels is operated, SBO pin can be used as a general port.

When SBO/SBI pin are connected for communication with 2 channels, SBO pin inputs/outputs serial data. The port direction control register switches input/output. At reception, set SC0SBIS of the SC0MD1 register always to “1”, and select “serial data input”. SBI pin can be used as a general port. (These are the same for serial interface 1.)

Set each flag as setup steps direct. Activate communication after setup of all control registers (Table 5-2-1: except for TXBUF and RXBUF) is completed.

Set the transfer clock by the SC0CKS register at transfer rate less than 2.5 MHz. (This is the same for serial interface 1.)

5-3-3 UART Serial Interface

Serial interface 0, 1 can be used for half-duplex UART communication. Table 5-3-12 shows UART serial interface functions.

Table 5-3-12 UART Serial Interface Functions

Communication style	UART (half-duplex)
Interrupt	Transmission, Reception
Used pins	TXD (I/O, shared use with SBO) RXD (I/O, shared use with SBI)
First transfer bit	MSB/LSB
Parity bit selection	√
Parity bit control	0 parity 1 parity Odd parity Even parity
Frame selection	7 bits + 1 STOP 7 bits + 2 STOPs 8 bits + 1 STOP 8 btis + 2 STOPs
Continuous operation	√
Maximum transfer rate	300 kbps (Baud rate timer (timer 3) is used.)

■ Activation Factor for Communication
At transmission, if any data is written to the transmission data buffer TXBUF, start condition is generated to start transfer. At reception, transfer is started by receiving start condition. If the data length of start bit “L” is longer than 0.5 bit, that can be generated as a start condition.

■ Transmission
Data transmission is automatically started by setting data to the transmission data buffer TXBUF. During transmission, reception and inputting start condition are impossible.

■ Reception
If start condition is recognized, reception is started after the transfer bit counter that counts transfer bit count is cleared. When start condition is received during communication, transfer bit counter is cleared. However, transmission is automatically restarted. Transmission is impossible during reception.

■ Transfer Bit Count Setup
The transfer bit count is automatically set after the frame mode is specified by the SC0FM1 to 0 flags of the SC0MD2 register. If the SC0CMD flag of the SC0MD1 register is set to “1” and UART communication is selected, setting of synchronous serial interface transfer bit count selection flags SC0LNG2 to 0 of the SC0MD0 register becomes disabled. (These are the same for serial interface 1.)

■ Input Edge/Output Edge Setup
The SC0CE1 to 0 flags of the SC0MD2 register set an output edge of the transmission data and an input edge of the reception data. Although transfer clock is not needed for UART communication, setting SC0CE1 to 0 flags is needed for determining the timing of data transmission/reception within this serial interface. At UART communication, set SC0CE1 to 0 flags always to “00”, and select falling for the transmission data output edge and rising for the reception data input edge. (These are the same for serial interface 1.)
Refer to Table 5-3-2 for detail about setting of input edge/output edge.

■ Data Input Pin Setup
The communication mode can be selected from with 2 channels (data output pin (TXD pin) and data input pin (RXD pin)) and with 1 channel (data I/O pin (TXD pin)). The RXD pin can be used only for serial data input. The TXD pin can be used for serial data input or output. The SC0IOM flag of the SC0MD1 register can specify which pin, RXD or TXD to input the serial data from. When “data input from TXD pin “ is selected to communicate with 1 channel, transmission and reception is switched by controlling direction with port I/O control register. At that time, the RXD pin is free to be used as a general port.

Set the SC0CS1 to 0 flags of the SC0MD0 register always to “00” in order to determine the timing of data transmission/reception within serial interface.

■ Frame Mode and Parity Check Setup

Figure 5-3-14 shows the data format at UART communication.

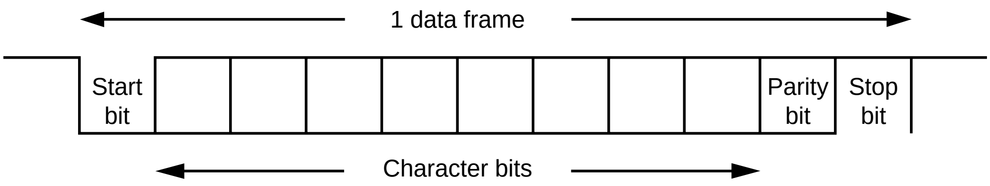


Figure 5-3-14 UART Serial Interface Transmission/Reception Data Format

The transmission/reception data consists of start bit, character bit, parity bit and stop bit. Table 5-3-13 shows its available kinds to be set.

Table 5-3-13 UART Serial Interface Transmission/Reception Data

Start bit	1 bit
Character bit	7, 8 bits
Parity bit	Fixed to 0, fixed to 1, even, odd, none
Stop bit	1, 2 bits

Frame mode is set by the SC0FM1 to 0 flags of the SC0MD2 register. Table 5-3-14 shows available kinds to be set. If the SC0CMD flag of the SC0MD1 register is set to “1” and UART communication is selected, transfer bit count of the SC0LNG2 to 0 flag of the SC0MD0 register becomes disabled. (These are the same for serial interface 1.)

Table 5-3-14 UART Serial Interface Frame Mode

SC0MD2 register		Frame mode
SC0FM1	SC0FM0	
0	0	Character bit 7 bits + Stop bit 1 bit
0	1	Character bit 7 bits + Stop bit 2 bit
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bit

Parity bit is to detect wrong bits of the transmission/reception data. Table 5-3-15 shows kinds of parity bit. Parity bit is set by the SC0NPE flag and SC0PM1 to 0 flags of the SC0MD2 register. (These are the same for serial interface 1.)

Table 5-3-15 Parity Bit of UART Serial Interface

SC0MD2 register			Parity bit	Setup
SC0NPE	SC0PM1	SC0PM0		
0	0	0	Fixed to 0	Set parity bit to "0".
0	0	1	Fixed to1	Set parity bit to "1".
0	1	0	Odd parity	Control the total number of "1" of parity bit and character bit to be odd.
0	1	1	Even parity	Control the total number of "1" of parity bit and character bit to be even.
1	-	-	None	Do not add parity bit.

■ Break Status Transmission Control Setup

The SC0BRKE flag of the SC0MD2 register can generate the break status. If set SC0BRKE to “1” to select the break transmission, all bits from start bit to stop bit transfer “0”.
(These are the same for serial interface 1.)

■ Reception Error

At reception, there are three types of errors: overrun error, parity error and framing error. Reception error can be determined by the SC0ORE flag, the SC0PEK flag and the SC0FEF flag of the SC0MD3 register. When even one of these errors is detected, the SC0ERE flag of the SC0MD3 register is set to “1”. The SC0PEK flag and the SC0FEF flag of these reception error flags are renewed at generation of communication complete interrupt SC0IRQ. Once the SC0ORE flag is set, it stays the same unless data of the reception data buffer RXBUF is read. Determine reception error flags by the end of the next communication. These error flags do not influence communication operation. Table 5-3-16 is the list of reception error source. (These are the same for serial interface 1.)

Table 5-3-16 Reception Error Source of UART Serial Interface

<table>
<tr><th>Flag</th><th>Error</th><th colspan="2">Error source</th></tr>
<tr><td>SC0ORE</td><td>Overrun error</td><td colspan="2">Next data is received before the reception buffer is read.</td></tr>
<tr><td rowspan="4">SC0PEK</td><td rowspan="4">Parity error</td><td>Fixed to 0</td><td>When parity bit is "1"</td></tr>
<tr><td>Fixed to 1</td><td>When parity bit is "0"</td></tr>
<tr><td>Odd parity</td><td>The total "1" of character bit and parity bit is even.</td></tr>
<tr><td>Even parity</td><td>The total "1" of character bit and parity bit is odd.</td></tr>
<tr><td>SC0FEF</td><td>Framing error</td><td colspan="2">Stop bit is not detected.</td></tr>
</table>

■ Judgement of Break Status Reception

Reception of break status can be judged. If all received data from start bit to stop bit is “0”, the SC0BRKF flag of the SC0MD2 register is set, which is judged to be break status. The SC0BRKF flag is set at generation of the reception complete interrupt SC0IRQ.
(These are the same for serial interface 1.)

■ Sequence Communication

This serial interface has sequence transfer function. If data is set to the transmission data buffer TXBUF during communication, the transmission buffer empty flag SC0TEMP is set to automatically make sequence communication. In this case, communication blank does not occur. Set data to TXBUF between data load to internal shift register and generation of communication complete interrupt SC0IRQ.
(These are the same for serial interface 1.)

■ Other Control Flags

The fallowing flags are not used at UART communication, so there is no need to set them.

Table 5-3-17 Other Control Flags

Register	Flag	Detail
SC0MD0	SC0LNG2 to 0	Selection of the transfer bit count
SC1MD0	SC1LNG2 to 0	
SC0MD1	SC0MST	Selection of clock master or clock slave
SC1MD1	SC1MST	

The following items are the same as in clock synchronous serial interface. Refer to Chapter 5 5-3-1 Clock Synchronous Serial Interface.

■ First Transfer Bit Setup

■ Transmission Data Buffer

■ Transmission Bit Count and First Transfer Bit

■ Reception Data Buffer

■ Reception Bit Count and First Transfer Bit

■ Reception Buffer Empty Flag Operation

■ Transmission Buffer Empty Flag Operation

■ BUSY Flag Operation

■ Transmission Timing

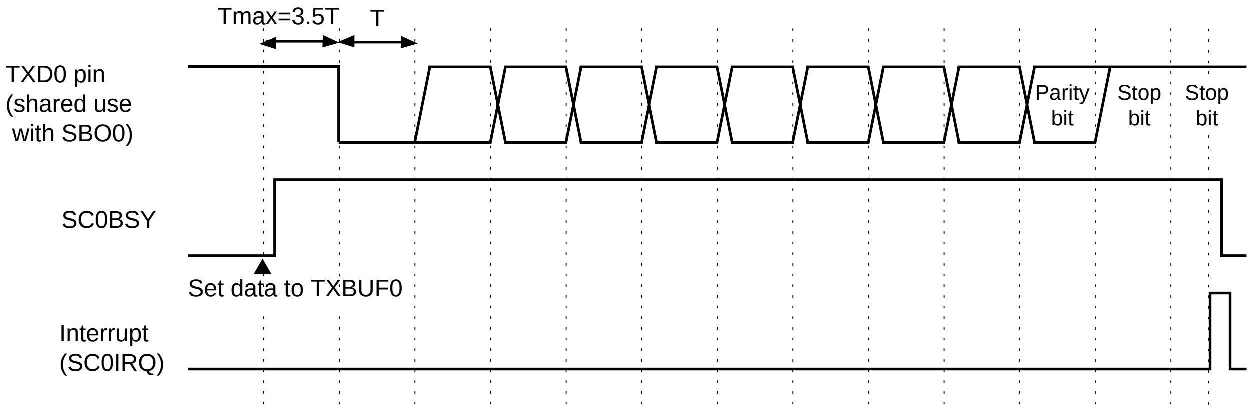


Figure 5-3-15 Transmission Timing (Parity Bit is Enabled.)

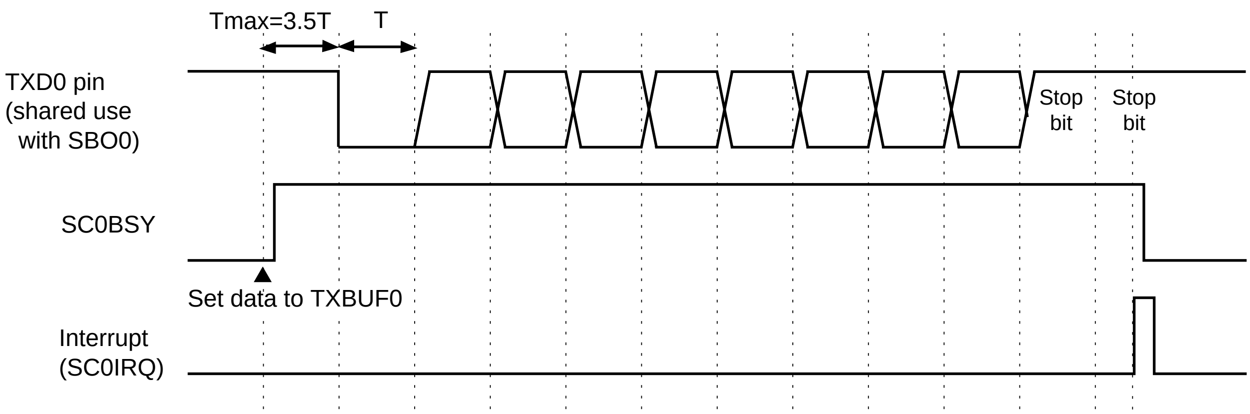


Figure 5-3-16 Transmission Timing (Parity Bit is Disabled.)

■ Reception Timing

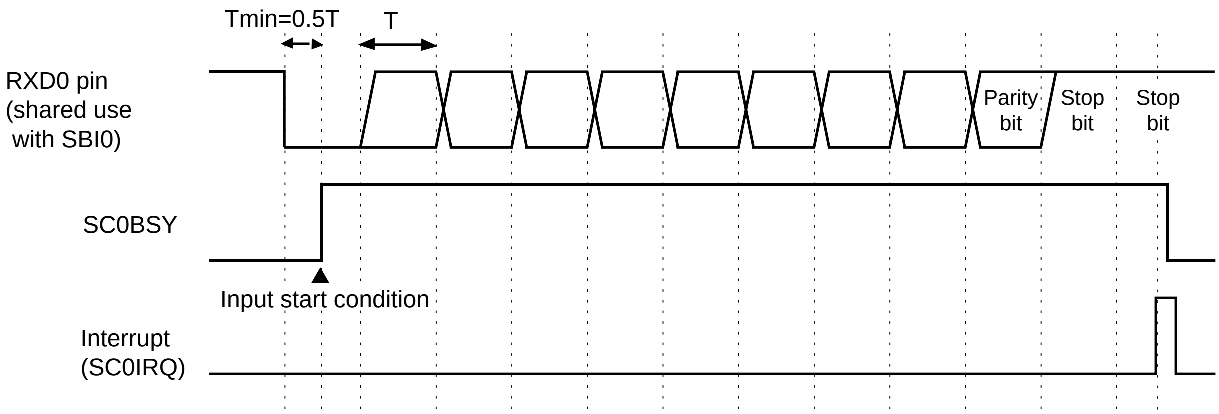


Figure 5-3-17 Reception Timing (Parity Bit is Enabled.)

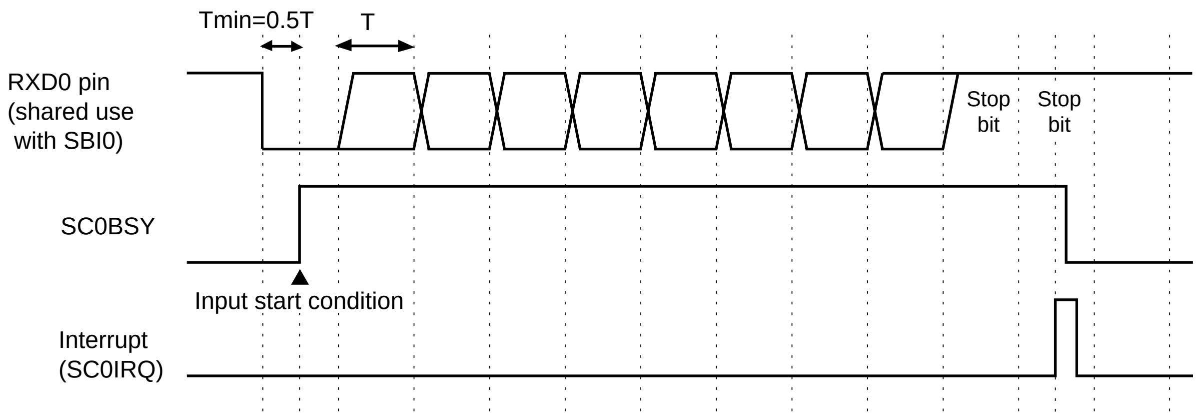


Figure 5-3-18 Reception Timing (Parity Bit is Disabled.)

■ Transfer Rate

Baud rate timer (Timer 3) can set any transfer rate. The setup example of the transfer rate is shown below. Refer to Chapter 4 4-2 8 Bit Timer (Timer 0 to 5) Setup Example for detail of baud rate timer setup.

At start-stop transmission, set transfer clock of serial interface to 16 times of transfer baud rate clock. The formula for baud rate is below.

baud rate (bps) = (original oscillation OSCI, OSCO $\times$ 4) Hz $\times$ 1/32 $\times$ 1/ Timer 3 dividing ratio

* System clock is used for Timer 3 source clock.

When the error in the above formula is within 2 %, communication is possible.

Baud rate settings at representative frequency are shown on the following page.

! Set the transfer rate within 300 kbps.

! At UART communication, set the SC0CKM flag of the SC0MD1 register to “1” and select “divided by 8”. (This is the same for serial interface 1.)

Table 5-3-18 Bit Rate Setting at Start-stop Transmission

(External ocsillation: 5 MHz, internal oscillation: 20 MHz)				
Baud rate	TM dividing	Real time	Error	
1200	520 *Note)	1201.92	0.16	
2400	260 *Note)	2403.85	0.16	
4800	130	4807.69	0.16	
9600	65	9615.38	0.16	
19200	33	18939.39	-1.36	
28800	22	28409.09	-1.36	
31250	20	31250.00	0.00	
38400	16	39062.50	1.73	
48000	13	48076.92	0.16	
57600	11	56818.18	-1.36	
76800	8	78125.00	1.73	
153600	4	156250.00	1.73	(Maximum)

*Note) When divinding ratio is more than 256, combination with Timer 0 or selection of clock source is needed.

Table 5-3-19 Bit Rate Setting at Start-stop Transmission

(External ocsillation: 4 MHz, internal oscillation: 16 MHz)				
Baud rate	TM dividing	Real time	Error	
1200	417 *Note)	1199.04	-0.08	
2400	208	2403.85	0.16	
4800	104	4807.69	0.16	
9600	52	9615.38	0.16	
19200	26	19230.77	0.16	
28800	17	29411.76	2.12	
31250	16	31250.00	0.00	
38400	13	38461.54	0.16	
48000	10	50000.00	4.17	
57600	9	55555.56	-3.55	
76800	7	71428.57	-6.99	
153600	3	166666.67	8.51	
250000	2	250000.00	0.00	(Maximum)

*Note) When divinding ratio is more than 256, combination with Timer 0 or selection of clock source is needed.

Table 5-3-20 Bit Rate Setting at Start-stop Transmission

(External ocsillation: 3 MHz, internal oscillation: 12 MHz)				
Baud rate	TM dividing	Real time	Error	
1200	312 *Note)	1201.92	0.16	
2400	156	2403.85	0.16	
4800	78	4807.69	0.16	
9600	39	9615.38	0.16	
19200	20	18750.00	-2.34	
28800	13	28846.15	0.16	
31250	12	31250.00	0.00	
38400	10	37500.00	-2.34	
48000	8	46875.00	-2.34	
57600	7	53571.43	-6.99	
76800	5	75000.00	-2.34	
153600	3	125000.00	-18.62	
187500	2	187500.00	0.00	(Maximum)

*Note) When divinding ratio is more than 256, combination with Timer 0 or selection of clock source is needed.

Table 5-3-21 Bit Rate Setting at Start-stop Transmission

(External ocsillation: 3 MHz, internal oscillation: 8 MHz)				
Baud rate	TM dividing	Real time	Error	
1200	208	1201.92	0.16	
2400	104	2403.85	0.16	
4800	52	4807.69	0.16	
9600	26	9615.38	0.16	
19200	13	19230.77	0.16	
28800	9	27777.78	-3.55	
31250	8	31250.00	0.00	
38400	7	35714.29	-6.99	
48000	5	50000.00	4.17	
57600	4	62500.00	8.51	
76800	3	83333.33	8.51	
125000	2	125000.00	0.00	(Maximum)

■ Pin Setup (1 Channel and 2 Channels, at Transmission)

Table 5-3-22 shows the pins setup at UART serial interface transmission. The pins setup is common to the TXD pin (shared use with the SBO pin) and the RXD pin (shared use with the SBI pin), regardless of independence or connection of those pins.

Table 5-3-22 UART Serial Interface Pins Setup (1 Channel and 2 Channels, at Transmission)

<table>
<tr><td rowspan="2">Setup item</td><td>Data output pin</td><td>Data input pin</td></tr>
<tr><td>TXD pin
(shared use with SBO)</td><td>RXD pin
(shared use with SBI)</td></tr>
<tr><td colspan="3">Serial interface 0</td></tr>
<tr><td>Pin</td><td>P02 (P62)</td><td>P01 (P61)</td></tr>
<tr><td rowspan="2">TXD/RXD pin</td><td colspan="2">TXD0/RXD0 independent or connected</td></tr>
<tr><td colspan="2">SC0MD1 (SC0IOM)</td></tr>
<tr><td rowspan="2">RXD input control</td><td rowspan="2">-</td><td>Input "1"</td></tr>
<tr><td>SC0MD1 (SC0SBIS)</td></tr>
<tr><td rowspan="2">Style</td><td>Push-pull/
Nch open-drain</td><td rowspan="2">-</td></tr>
<tr><td>SC0CKS (SC0ODC1)</td></tr>
<tr><td>Port</td><td colspan="2">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
<tr><td colspan="3">Serial interface 1</td></tr>
<tr><td>Pin</td><td>P65</td><td>P64</td></tr>
<tr><td rowspan="2">TXD/RXD pin</td><td colspan="2">TXD1/RXD1 independent or connected</td></tr>
<tr><td colspan="2">SC1MD1 (SC1IOM)</td></tr>
<tr><td rowspan="2">RXD input control</td><td rowspan="2">-</td><td>Input "1"</td></tr>
<tr><td>SC1MD1 (SC1SBIS)</td></tr>
<tr><td rowspan="2">Style</td><td>Push-pull/
Nch open-drain</td><td rowspan="2">-</td></tr>
<tr><td>SC1CKS (SC1ODC1)</td></tr>
<tr><td>Port</td><td colspan="2">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
</table>

■ Pin Setup (2 Channels, at Reception)

Table 5-3-23 shows the pins setup at UART serial interface reception with 2 channels (the TXD pin and the RXD pin).

Table 5-3-23 UART Serial Interface Pins Setup (2 Channels, at Reception)

Setup item	Data output pin TXD pin (shared use with SBO)	Data input pin RXD pin (shared use with SBI)
Serial inteface 0		
Pin	P02 (P62)	P01 (P61)
TXD/RXD pin	TXD0/RXD0 independent SC0MD1 (SC0IOM)	
RXD input control	-	Serial data input SC0MD1 (SC0SBIS)
Style	-	-
Port	Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.	
Serial interface 1		
Pin	P65	P64
TXD/RXD pin	TXD1/RXD1 independent SC1MD1 (SC1IOM)	
RXD input control	-	Serial data input SC1MD1 (SC1SBIS)
Style	-	-
Port	Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.	

■ Pin Setup (1 Channel, at Reception)

Table 5-3-24 shows the pins setup at UART serial interface reception with 1 channel (the TXD pin). The RXD pin is free to be used as a port.

Table 5-3-24 UART Serial Interface Pins Setup (1 Channel, at Reception)

<table>
<tr><td rowspan="2">Setup item</td><td>Data output pin</td><td>Serial unused pin</td></tr>
<tr><td>TXD pin
(shared use with SBO)</td><td>RXD pin
(shared use with SBI)</td></tr>
<tr><td colspan="3">Serial inteface 0</td></tr>
<tr><td>Pin</td><td>P02 (P62)</td><td>P01 (P61)</td></tr>
<tr><td rowspan="2">TXD/RXD pin</td><td colspan="2">TXD0/RXD0 connected</td></tr>
<tr><td colspan="2">SC0MD1 (SC0IOM)</td></tr>
<tr><td rowspan="2">RXD input control</td><td rowspan="2">-</td><td>Serial data input</td></tr>
<tr><td>SC0MD1 (SC0SBIS)</td></tr>
<tr><td>Style</td><td>-</td><td>-</td></tr>
<tr><td>Port</td><td colspan="2">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
<tr><td colspan="3">Serial inteface 1</td></tr>
<tr><td>Pin</td><td>P65</td><td>P64</td></tr>
<tr><td rowspan="2">TXD/RXD pin</td><td colspan="2">TXD1/RXD1 connected</td></tr>
<tr><td colspan="2">SC1MD1 (SC1IOM)</td></tr>
<tr><td rowspan="2">RXD input control</td><td rowspan="2">-</td><td>Serial data input</td></tr>
<tr><td>SC1MD1 (SC1SBIS)</td></tr>
<tr><td>Style</td><td>-</td><td>-</td></tr>
<tr><td>Port</td><td colspan="2">Refer to Chapter 7 Port Function about port I/O control, output mode control and pull-up setup.</td></tr>
</table>

5-3-4 Setup Example

■ Transmission Setup

The setup example at UART transmission with serial interface 0 is shown. Table 5-3-25 shows the conditions at transmission.

Table 5-3-25 UART Interface Transmission Setup

Setup item	Set to
TXD0/RXD0 pin	Connected (with 1 channel)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	Timer 3 output
TXD0 pin type	Nch open-drain
Pull-up resistor of serial pin	Added
Parity bit add/check	"0" add/check
Serial 0 communication complete interrupt	Enable

An example setup procedure with a description of each step is shown below.

Setup Procedure	Description
(1) Set pins. P0MD (x'00FFF0') bp3 : P0MD3 = 1 P0DIR (x'00FFE0') bp2 : P0DIR2 = 1 PMSEL (x'00FFA0') bp2 : PMSEL2 = 0	(1) With the P0MD register, the P0DIR register and the PMSEL register, set P02 to the UART serial data output pin TXD0 (shared use with the SBO0 pin).
(2) Set the interrupt. G3ICR (x'00FC46') bp14-12 : G3LV2-0 = 100 bp10 : SC0IE = 1 bp6 : SC0IR = 0 (bp15-0 = x'4400')	(2) Enable the interrupt. At this time, erase all prior interrupt requests. That is set interrupt level (6 to 0) to G3LV2-0 of the maskable interrupt control register (group) 3 (G3ICR), and also set '1' to SC0IE and '0' to SC0IR. For example, write x'4400' to G3ICR. After this, when transmission of serial interface 0 is completed, the interrupt is occurred.
(3) Select the clock source. SC0CKS (x'00FD84') bp2-0 : SC0CS1-0 = 11	(3) Set the SC0CS1-0 flags of the SC0CKS register to "11" and select 2 dividing of Timer 3 output for the clock source.

Setup Procedure	Description
(4) Control the pin type. SC0CKS (x'00FD84') bp3 : SC0ODC1 = 1 PPUPA (x'00FFB0') bp7 : PPUPA7 = 1	(4) Set the SC0ODC1 flag of the SC0CKS register to "1" to select Nch open-drain for TXD0 pin type. Set the PPUPA7 flag of the PPUPA register to "1" to select "add pull-up resistor" for serial interface pin.
(5) Select the start condition. SC0MD0 (x'00FD80') bp3 : SC0STE = 1	(5) Set the SC0STE flag of the SC0MD0 register to "1" to enable start condition.
(6) Select the first bit to be transferred. SC0MD0 (x'00FD80') bp4 : SC0DIR = 0	(6) Set the SC0DIR flag of the SC0MD0 register to "0" to set MSB as a transfer first bit.
(7) Control the output data. SC0MD2 (x'00FD82') bp0 : SC0BRKE = 0	(7) Set the SC0BRKE flag of the SC0MD2 register to "0" to select serial data transmission.
(8) Select the added parity bit. SC0MD2 (x'00FD82') bp3 : SC0NPE = 0 bp5-4 : SC0PM1-0 = 00	(8) Set the SC0PM1-0 flags of the SC0MD2 register to "00" to select 0 parity, and set the SC0NPE flag to "0" to add parity bit.
(9) Specify the frame mode. SC0MD2 (x'00FD82') bp7-6 : SC0FM1-0 = 11	(9) Set the SC0FM1-0 flags of the SC0MD2 register to "11" to select 8 bits + 2 stop bits for the frame mode.
(10) Select the communication type. SC0MD1 (x'00FD81') bp0 : SC0CMD = 1	(10) Set the SC0CMD flag of the SC0MD1 register to "1" to select half-duplex UART.
(11) Select the clock dividing. SC0MD1 (x'00FD81') bp3 : SC0CKM = 1	(11) Set the SC0CKM flag of the SC0MD1 register to "1" to divide the clock source by 8.
(12) Control the pin function. SC0MD1 (x'00FD81') bp5 : SC0SBIS = 0 bp7 : SC0IOM = 1	(12) Set the SC0SBIS flag of the SC0MD1 register to "0" and SC0IOM flag to "1", which makes the RXD0 pin serve as a general port.

Setup Procedure	Description
(13) Set the baud rate timer (Timer 3):1 TM3MD (x'00FE23') bp7 : TM3EN = 0 bp6 : TM3LD = 0 bp1-0 : TM3S1-0 =11	(13) Set both the TM3EN flag and the TM3LD flag of the TM3MD register to “0” to stop the count operation. Set the TM3S1-0 flags to “11” to select SYSCLK for clock source.
(14) Set the baud rate timer (Timer 3):2 TM3BR (x'00FE13') bp7-0 : TM3BR7-0 = 01000000 (x’40’)	(14) Set baud rate 9600 bps original oscillation 5 MHz as an example here. Baud rate = (original oscillation $\times$ 4) $\times$ (1/32) $\times$ (1/divisor of Timer 3), which means that 9600 = (5M $\times$ 4) $\times$ (1/32) $\times$ (1/divisor of Timer 3) The divisor of Timer 3 is 65.10, so set 64 of 65-1 for the base register of the Timer 3.
(15) Set the baud rate timer (Timer 3):3 TM3MD (x'00FE23') bp6 : TM3LD = 1 TM3MD (x’00FE23’) bp6 : TM3LD = 0 TM3MD (x’00FE23’) bp7 : TM3EN = 1	(15) Set the TM3LD flag of the TM3MD register to “1” to load the value of the base register. Then clear the TM3LD flag to “0”, and set the TM3EN flag to “1” to start the timer operation. If this order is not kept, binary counter can not be counted at the first count.
(16) Start the serial interface transmission. Transmission data $\rightarrow$ TXBUF0(x’00FD87’)	(16) When the transmission data is set to the serial interface transmission data buffer (TXBUF0), transmission is started. When transmission is completed, serial interface 0 transfer complete interrupt (SC0IRQ) is generated.

Note: (5) and (6) can be set at the same time, so can (7) to (9), and (10) to (12).

When the TXD/RXD pins are connected for communication with 1 channel, input and output serial data from the TXD pin. The port direction control register switches input/output. The RXD pin can be used as a general port.

Set each flag as setup steps direct. Activate communication after setup of all control registers (Table 5-2-1: except for TXBUF and RXBUF) is completed.

Timer that can be used as a baud rate timer is only Timer 3.

■ Reception Setup

The setup example at UART reception with serial interface 1 is described below. Table 5-3-26 shows the conditions at reception.

Table 5-3-26 UART Interface Reception Setup

Setup item	Set to
TXD1/RXD1 pin	Connected (with 1 channel)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	Timer 3 output
TXD1 pin type	Nch open-drain
Pull-up resistor of serial pin	Added
Parity bit add/check	"0" add/check
Serial 1 communication complete interrupt	Enable

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set pins. P6MDB (x'00FFFB') b1-0 : P6MDB1-1 = 10 P6DIR (x'00FFE6') bp5 : P6DIR5 = 0	(1) With the P6MDB register and the P6DIR register, set P65 to the UART serial data input pin TXD1 (shared use with the SBO1 pin).
(2) Set the interrupt. G4ICR (x'00FC48') bp14-12 : G4LV2-0 = 100 bp10 : SC1IE = 1 bp6 : SC1IR = 0 (bp15-0 = x'4400')	(2) Enable the interrupt. At this time, erase all prior interrupt requests. That is set interrupt level (6 to 0) to G4LV2-0 of the maskable interrupt control register (group) 4 (G4ICR), and also set '1' to SC1IE and '0' to SC1IR. For example, write x'4400' to G4ICR. After this, when transmission of serial interface 1 is completed, the interrupt is occurred.
(3) Select the clock source. SC1CKS (x'00FD94') bp2-0 :SC1CS1-0 = 11	(3) Set the SC1ODC1 flag of the SC1CKS register to "1" and select 2 dividing of Timer 3 output for the clock source.
(4) Control the pin type. SC1CKS (x'00FD94') bp3 : SC1ODC1 = 1 PPUPC (x'00FFB2') bp2 : PPUPC2 = 1	(4) Set the SC1ODC1 flag of the SC1CKS register to "1" to select Nch open-drain for TXD1 pin type. Set the PPUPC2 flag of the PPUPC register to "1" to select "add pull-up resistor" for serial interface pin.

Setup Procedure	Description
(5) Select the start condition. SC1MD0 (x'00FD90') bp3 : SC1STE = 1	(5) Set the SC1STE flag of the SC1MD0 register to “1" to enable start condition.
(6) Select the first bit to be transferred. SC1MD0 (x'00FD90') bp4 : SC1DIR = 0	(6) Set the SC1DIR flag of the SC1MD0 register to “0” to set MSB as a transfer first bit.
(7) Select the added parity bit. SC1MD2 (x’00FD92’) bp3 : SC1NPE = 0 bp5-4 : SC1PM1-0 = 00	(7) Set the SC1PM1-0 flags of the SC1MD2 register to “00“ to select 0 parity, and set the SC1NPE flag to “0” to add parity bit.
(8) Specify the frame mode. SC1MD2 (x’00FD92’) bp7-6 : SC1FM1-0 = 11	(8) Set the SC1FM1-0 flags of the SC1MD2 register to “11” to select 8 bits + 2 stop bits.
(9) Select the communication type. SC1MD1 (x’00FD91’) bp0 : SC1CMD = 1	(9) Set the SC1CMD flag of the SC1MD1 register to “1” to select half-duplex UART.
(10) Select the clock dividing. SC1MD1 (x’00FD91’) bp3 : SC1CKM = 1	(10) Set the SC1CKM flag of the SC1MD1 register to “1” to divide the clock source by 8.
(11) Control the pin function. SC1MD1 (x’00FD91’) bp5 : SC1SBIS = 1 bp7 : SC1IOM = 1	(11) Set the SC1SBIS flag of the SC1MD1 register to “1” to select serial data input. Set SC1IOM flag to “1”, which makes the RXD1 pin serve as a general port.
(12) Set the baud rate timer (Timer 3):1 TM3MD (x'00FE23') bp7 : TM3EN = 0 bp6 : TM3LD = 0 bp1-0 : TM3S1-0 =11	(12) Set both the TM3EN flag and the TM3LD flag of the TM3MD register to “0” to stop the count operation. Set the TM3S1-0 flags to “11” to select SYSCLK for clock source.

Setup Procedure	Description
(13) Set the baud rate timer (Timer 3):2 TM3BR (x'00FE13') bp7-0 : TM3BR7-0 = 01000000 (x'40')	(13) Set baud rate 9600 bps original oscillation 5 MHz as an example here. Baud rate = (original oscillation $\times$ 4) $\times$ (1/32) $\times$ (1/divisor of Timer 3), which means that 9600 = (5M $\times$ 4) $\times$ (1/32) $\times$ (1/divisor of Timer 3) The divisor of Timer 3 is 65.10, so set 64 of 65-1 for the base register of the Timer 3. Set “01000000” (x’40’) to the TM3BR register.
(14) Set the baud rate timer (Timer 3):3 TM3MD (x'00FE23') bp6 : TM3LD = 1 TM3MD (x’00FE23’) bp6 : TM3LD = 0 TM3MD (x’00FE23’) bp7 : TM3EN = 1	(14) Set the TM3LD flag of the TM3MD register to “1” to load the value of the base register. Then clear the TM3LD flag to “0”, and set the TM3EN flag to “1” to start the timer operation. If this order is not kept, binary counter can not be counted at the first count.
(15) Start the serial interface transmission. Transmission data $\rightarrow$ Input to the TXD1 pin	(15) When serial data is input from the TXD1 pin and start condition is recognized, the reception data is captured in the serial interface reception data buffer RXBUF 1. When transmission is completed, serial interface 1 transfer complete interrupt SC1IRQ is generated.

Note: (5) and (6) can be set at the same time, so can (7) and (8), and (9) to (11).

When the TXD/RXD pins are connected for communication with 1 channel, input and output serial data from the TXD pin. The port direction control register switches input/output. At reception, set SC1SBIS of the SC1MD1 register always to “1” and select “serial data input”. The RXD pin can be used as a general port. (These are the same for serial interface 0.)

Set each flag as setup steps direct. Activate communication after setup of all control registers (Table 5-2-1: except for TXBUF and RXBUF) is completed.

Timer that can be used as a baud rate timer is only Timer 3.

Chapter 6 Analog Interface

6-1 Analog Interface

6-1-1 Overview

This LSI series contains a 10-bit charge redistribution A/D converter. The A/D converter supports digital signal processing in the voice and audio frequency ranges with a 10-bit resolution, a minimum conversion time of 11.2 µs (at 5 MHz external oscillation) and a low current A/D converter.

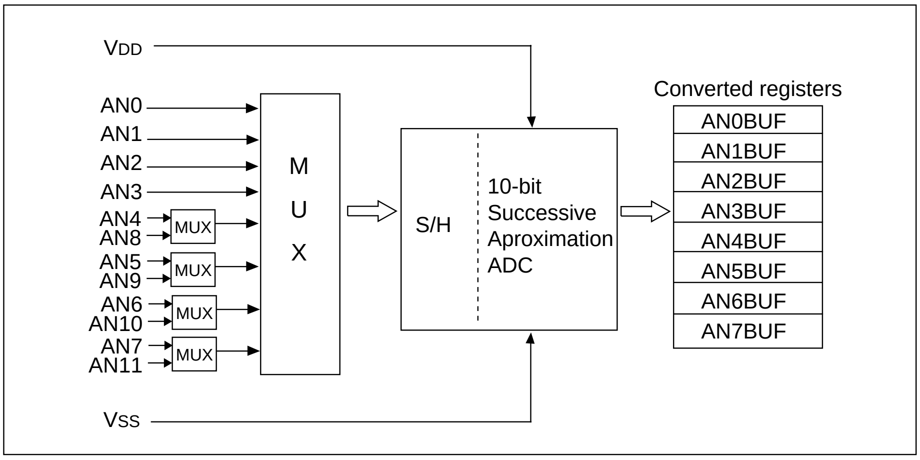


Figure 6-1-1 Analog Interface Configuration

To secure the accuracy of A/D conversion, be sure to keep right notices during A/D converting.

■ Notices When Using A/D Converter

(1) Set the impedance of the analog signal for A/D conversion to 8 kΩ or less.

(2) Connect the A/D input pin to the condenser of 2000 pF or more to control the voltage change of the A/D input pin if the impedance of the analog signal cannot be set to 8 kΩ or less.

(3) To prevent the power potential fluctuation, do not change the chip output level from high level to low level or vice verse, or do not switch the peripheral load circuit on/off during A/D conversion.

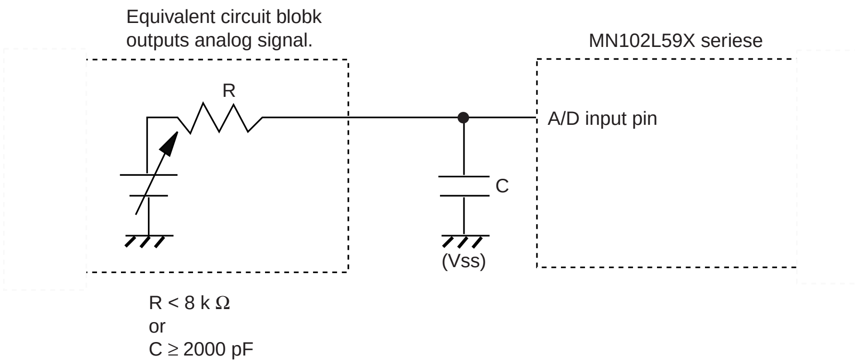


Figure 6-1-2 Connection of A/D Conversion Input Signal

Table 6-1-1 A/D Converter Functions

Feature	Description
S/H	Built-in
Conversion Resolution	10-bit ± 3 LSB (AN0 to AN3) 10-bit ± 4 LSB (AN4 to AN 11) The A/D converter converts the voltage between V_{DD} and V_{SS} devided into 1024 and this converted result is stored in AN7BUF to AN0BUF.
Conversion Time	11.2 µs or more per channel (sample time 800 ns with 5-MHz external oscillation)
Clock Source	Internal system clock SYSCLK divided by 1, 2, 4, 8, and 16
Operating Mode	30 operating mode: Single conversion of single channel (channel 0 to channel 7) Single conversion of multiple channels (channel 0 to channel 1, channel 0 to channel 2, channel 0 to channel 3, channel 0 to channel 4, channel 0 to channel 5, channel 0 to channel 6, channel 0 to channel 7) Continuous conversion of single channel (channel 0 to channel 7) Continuous conversion of multiple channels (channel 0 to channel 1, channel 0 to channel 2, channel 0 to channel 3, channel 0 to channel 4, channel 0 to channel 5, channel 0 to channel 6, channel 0 to channel 7)
Conversion Start	Timer 1 underflow, TM11 PWMST or register setting by instruction
Interrupt	An interrupt occures each time the conversion sequence ends.

ANn pin corresponds to the channel number. For example, the AN3 pin corresponds to channel 3.

Select from AN4 to AN7 or AN8 to AN11 independently to connect them to ch4 to ch7.

■ Selecting the A/D Converter Clock Source

The A/D converter clock source is selected from SYSCLK, SYSCLK/2, SYSCLK/4, SYSCLK/8 or SYSCLK/16 as the conversion speed is 11.2 µs or more. Select the A/D converter clock source as follows:

SYSCLK frequency/divisor ≤ 2.5 MHz

For example, select the A/D converter clock source as SYSCLK/8 (the conversion speed of 11.2 µs) or SYSCLK/16 (the conversion speed of 22.4 µs) with 5-MHz external oscillation, and select SYSCLK/4, SYSCLK/8 or SYSCLK/16 with 2.5-MHz external oscillation.

The conversion time is 14 cycles of the A/D converter clock source as Figure 6-1-3 shows. For example, the conversion time (s) is calculated as follows when SYSCLK/4 is selected.

SYSCLK cycle (s) × 4 (dividing) × 14 (cycle)

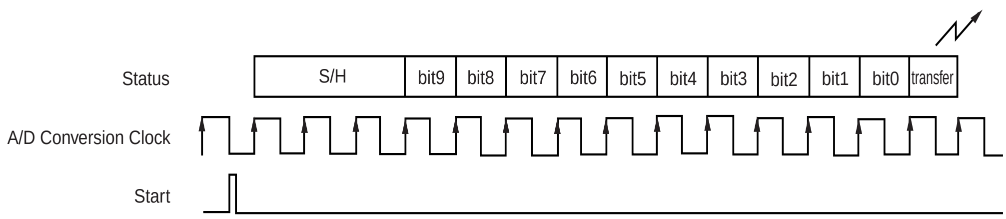


Figure 6-1-3 A/D Conversion Timing

■ One Channel/Single Conversion

The A/D converter converts one A/D input signal of 1 channel once. An A/D interrupt occurs as soon as the conversion ends. Set the channel to be converted to AN1CH[2:0] bits.

Set the ANST flag (that starts timer conversion) and the ANEN flag (that starts and executes conversion) to ‘0’ and ‘1’ respectively when the conversion starts using the ANEN flag. The ANEN flag becomes ‘1’ during the conversion and ‘0’ after the conversion ends.

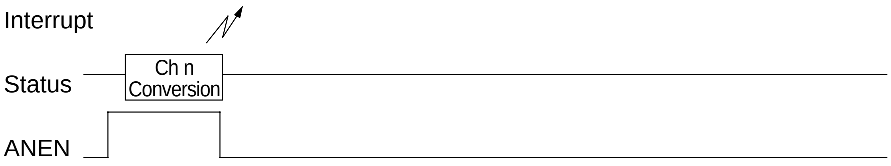


Figure 6-1-4 One Channel/Single Conversion Timing

■ Multiple Channels/Single Conversion

The A/D converter converts A/D input signals of continuous channels from channel 0 once. An A/D interrupt occurs as soon as the conversion for all channels ends. Set AN1CH[2:0] bits to channel 0 and the ANNCH flag to the last channel to be converted. (The conversion starts from channel 0.)

Set the ANST flag and the ANEN flag to ‘0’ and ‘1’ respectively when the conversion starts using the ANEN flag. The ANEN flag becomes ‘1’ during the conversion and ‘0’ after all the conversion sequence ends. In addition, the AN1CH[2:0] bits are set to the channel number during the conversion and ‘0’ after all the conversion sequence ends.

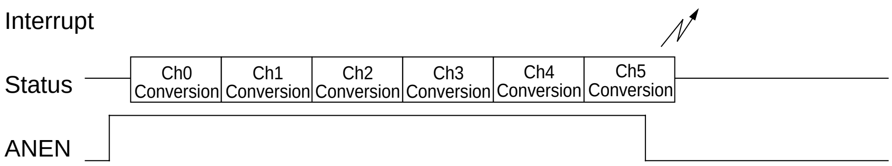


Figure 6-1-5 Multiple Channels/Single Conversion Timing

■ One Channel/Continuous Conversion

The A/D converter converts one A/D input signal continuously. An A/D interrupt occurs each time the conversion ends. Set AN1CH[2:0] bits to the channel number to be converted.

Set the ANST flag and the ANEN flag to '0' and '1' respectively when the conversion starts using the ANEN flag. Setting forcibly the ANEN flag to '0' ends the conversion.

ANNCH is ignored.

AN1CH, ANNCH, ANEN and ANST are the flags of the A/D conversion control register (ANCTR).

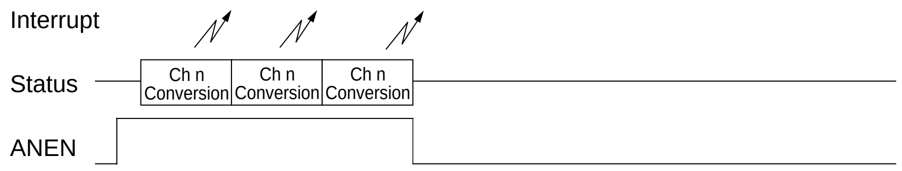


Figure 6-1-6 One Channel/Continuous Conversion Timing

■ Multiple Channels/Continuous Conversion

The A/D converter converts A/D input signals of continuous channels from channel 0 continuously. An A/D interrupt occurs each time the continuous conversion ends. Set AN1CH[2:0] bits to channel 0 and the ANNCH flag to the last channel to be converted. (The conversion starts from channel 0.)

Set the ANST flag and the ANEN flag to '0' and '1' respectively when the conversion starts using the ANEN flag. Setting forcibly the ANEN flag to '0' ends the conversion. The ANEN flag becomes '1' during the conversion and '0' after all the conversion sequence ends. The AN1CH[2:0] bits are set to the channel number during the conversion and '0' after all the conversion sequence ends.

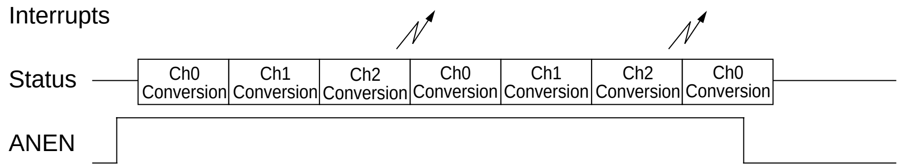


Figure 6-1-7 Multiple Channels/Continuous Conversion Timing

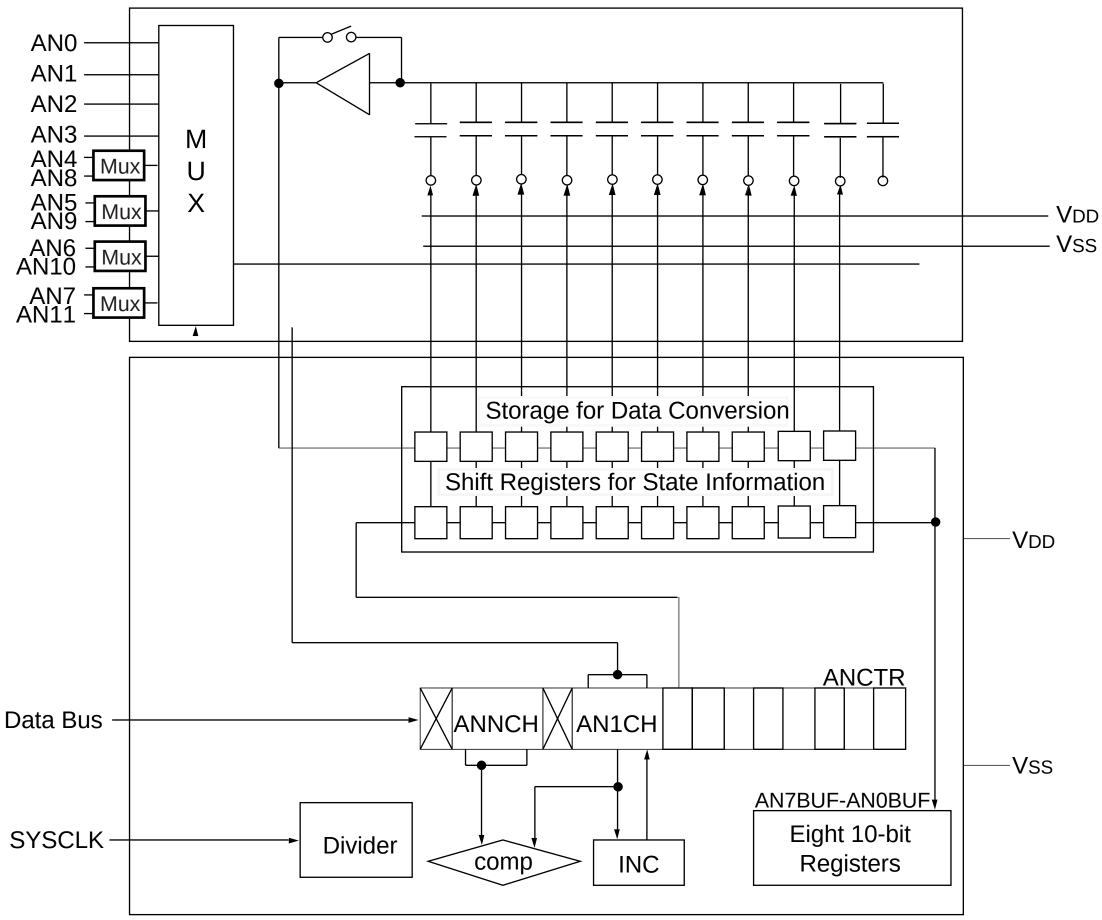


Figure 6-1-8 Analog Interface Block Diagram

6-1-2 Control Registers

The A/D converter contains the A/D conversion control register (ANCTR) and the A/D conversion data registers (ANnBUF) corresponding to channel 7 to channel 0 (AN11 pin to AN0 pin).

Table 6-1-2 List of A/D Conversion Control Registers

Control register	A/D control register (ANCTR), x'00FDB0'	
Data register	A/D 0 conversion data buffer (ch 0) (AN0BUF), x'00FDC0'	A/D 4 conversion data buffer (ch 4) (AN4BUF), x'00FDC8'
	A/D 1 conversion data buffer (ch 1) (AN1BUF), x'00FDC2'	A/D 5 conversion data buffer (ch 5) (AN5BUF), x'00FDCA'
	A/D 2 conversion data buffer (ch 2) (AN2BUF), x'00FDC4'	A/D 6 conversion data buffer (ch 6) (AN6BUF), x'00FDCC'
	A/D 3 conversion data buffer (ch 3) (AN3BUF), x'00FDC6'	A/D 7 conversion data buffer (ch 7) (AN7BUF), x'00FDCE'
Port selection register	Analog port selection register (ANSEL), x'00FFA2'	

The A/D conversion control register (ANCTR) sets the A/D conversion operating conditions.

The A/D conversion results for channel 7 to channel 0 (AN11 pin to AN0 pin) are input to the A/D conversion data registers (ANnBUF), so writing is impossible. The default value is unstable.

The port selection register (ANSEL) sets ports used as analog pins.

6-2 Setup Examples

6-2-1 One Channel A/D Conversion Using AN6 Pin

This section describes the one channel A/D conversion setup by software. The AN6 pin inputs the analog voltage (0 V to 5 V) and obtains the A/D conversion result.

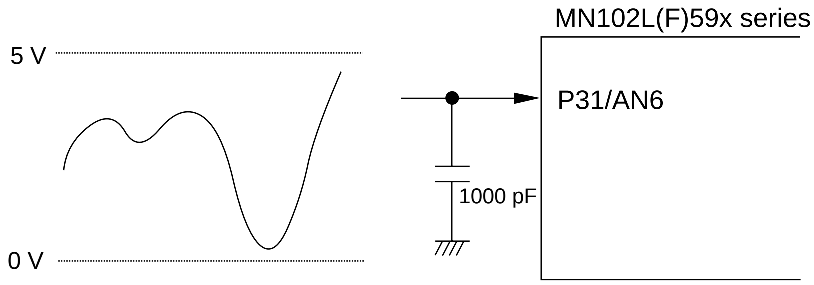


Figure 6-2-1 One Channel A/D Conversion

■ Pins Setup

(1) Set port P31 as the analog input AN6 by the analog port selection register (ANSEL) and the multi-port selection register (PMSEL). (Set ANSEL1 to '1' and PMSEL10 to '0'.)

ANSEL: x'00FFA2'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	AN SEL11	AN SEL10	AN SEL9	AN SEL8	AN SEL7	AN SEL6	AN SEL5	AN SEL4	AN SEL3	AN SEL2	AN SEL1	AN SEL0
				0	0	0	0	0	0	0	0	0	0	1	0

PMSEL: x'00FFA0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	PM SEL11	PM SEL10	PM SEL9	PM SEL8	PM SEL7	PM SEL6	PM SEL5	PM SEL4	PM SEL3	PM SEL2	PM SEL1	PM SEL0
				0	0	0	0	0	0	0	0	0	0	0	0

■ A/D Conversion Control Register Setup

(2) Set the operation mode to the A/D conversion control register (ANCTR). Set ANMD to 1ch/single conversion and the clock source to SYSCLK/4 (10 MHz/4 with 5-MHz external oscillation). Set ANEN to ‘0’ and AN1CH[2:0] to the channel number to be converted (ch6).

ANCTR: x’00FDB0’

ANNCH is ignored.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	AN NCH2	AN NCH1	AN NCH0	—	AN 1CH2	AN 1CH1	AN 1CH0	AN EN	AN ST1	AN ST0	AN CK2	AN CK1	AN CK0	AN MD1	AN MD0
-	0	0	0	-	1	1	0	0	0	0	-	0	0	0	0

(3) Set the ANEN flag to ‘1’ to start the conversion. Conversion starts on the rising edge of the first A/D conversion clock source that set ANEN to ‘1’. The conversion time is 14 cycles of the A/D conversion clock source (5.6 µs, 5.6 µs to 6.0 µs after ANEN is set).

Set the ANEN flag to ‘1’ when starting the A/D conversion by software.

(4) Wait for the conversion to end. ANEN flag is ‘1’ during the conversion and cleared to ‘0’ after the conversion ends. The program waits until the ANEN flag is cleared to ‘0’.

The CPU can read the conversion result by generating an interrupt. In this case, the CPU does not need to wait until the ANEN flag is set because an interrupt occurs after the conversion result is stored in AN6BUF.

(5) Read the AN6 conversion data buffer (AN6BUF).
The converter divides 0 V to 5 V into 1024 and the conversion result is the value from 0 to 1023.

AN6BUF: x’00FDCC’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	AN6 BUF9	AN6 BUF8	AN6 BUF7	AN6 BUF6	AN6 BUF5	AN6 BUF4	AN6 BUF3	AN6 BUF2	AN6 BUF1	AN6 BUF0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

6-2-2 Multiple Channels A/D Conversion Using AN2 to AN0 Pins

The AN2, AN1 and AN0 pins input the analog voltage of 0 V to 5 V and obtains the A/D conversion results. The converter performs periodically using timer 1.

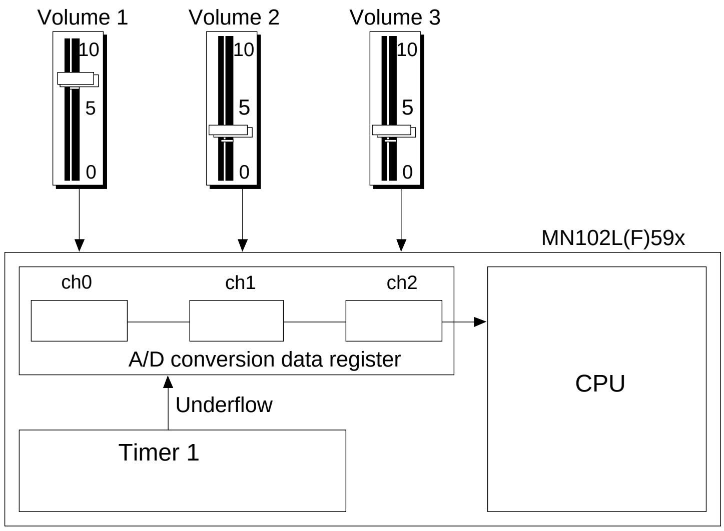


Figure 6-2-2 Multiple Channel A/D Conversion

■ Pins Setup

(1) Set ports P35 to P37 as the analog input pins AN2 to AN0 by the analog port selection register (ANSEL). (Set ANSEL7 to ANSEL5 to ‘1’.)

ANSEL: x’00FFA2’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	AN SEL11	AN SEL10	AN SEL9	AN SEL8	AN SEL7	AN SEL6	AN SEL5	AN SEL4	AN SEL3	AN SEL2	AN SEL1	AN SEL0
				0	0	0	0	1	1	1	0	0	0	0	0

■ A/D Conversion Control Register Setup

(2) Set the operation mode to the A/D conversion control register (ANCTR). Set ANMD to multiple channel/single conversion and the ANCK[1:0] bits to SYSCLK/4 (10 MHz/4 with 5-MHz external oscillation). Set ANEN and ANST0 to ‘0’, and ANST1 to ‘1’. Set AN1CH[2:0] to the first channel number to be converted (channel 0) and ANNCH[2:0] to the last channel number to be converted (channel 2).

ANCTR: x’00FDB0’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	AN NCH2	AN NCH1	AN NCH0	—	AN 1CH2	AN 1CH1	AN 1CH0	AN EN	AN ST1	AN ST0	AN CK2	AN CK1	AN CK0	AN MD1	AN MD0
-	0	1	0	-	0	0	0	0	1	0	0	1	0	0	1

■ Timer 1 Setup (Conversion Cycle Setup)

(3) Set the timer 1 divisor. When timer 1 divides SYSCLK by 256, set the timer 1 base register (TM1BR) to 255. (The valid range for TM1BR is 1 to 255.)

TM1BR: x'00FE11'

7	6	5	4	3	2	1	0
TM1 BR7	TM1 BR6	TM1 BR5	TM1 BR4	TM1 BR3	TM1 BR2	TM1 BR1	TM1 BR0
1	1	1	1	1	1	1	1

(4) Load the TM1BR value to TM1BC. To do this, set TM1LD and TM1EN of Timer 1 mode register (TM1MD) to ‘1’ and ‘0’ respectively. At the same time, select the clock source.

Do not change the clock source after this step. Changing the clock source while controlling count operation will corrupt the binary counter value.

TM1MD: x'00FE21'

7	6	5	4	3	2	1	0
TM1 EN	TM1 LD	—	—	—	—	TM1 S1	TM1 S0
0	1	-	-	-	-	1	0

(5) Set both TM1LD and TM1EN of the TM1MD register to ‘0’.

If this setting is omitted, the timer 1 binary counter may not start at the first cycle.

(6) Set both TM1LD and TM1EN to ‘0’. This starts timer 1. Counting starts at the beginning of the next cycle.

The periodical A/D conversion saves the power consumption compared to the continuous conversion.

When the timer 1 binary counter (TM1BC) reaches 0, as soon as it loads the value of 255 from the timer 1 base register (TM1BR) at the next count, a timer 1 underflow interrupt request occurs. The A/D converter converts each ch2, ch1 and ch0 once when timer 1 underflows.

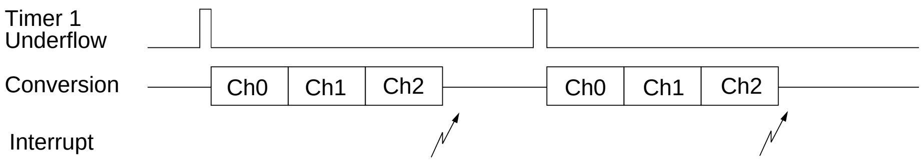


Figure 6-2-3 A/D Conversion Timing
(Single Conversion Each of Channel 2 to Channel 0)

Chapter 7 Ports

7

7-1 Ports

7-1-1 Overview

This LSI series contains eight I/O ports. Ports 0 is 3 bits, port 1 is 7 bits, port 2, port 4 and port 6 are 6 bits, and port 3, port 5 and port 7 are 8 bits. All ports are bidirectional. All ports can control the I/O direction in bit unit.

Table 7-1-1 Port Functions (1 of 7)

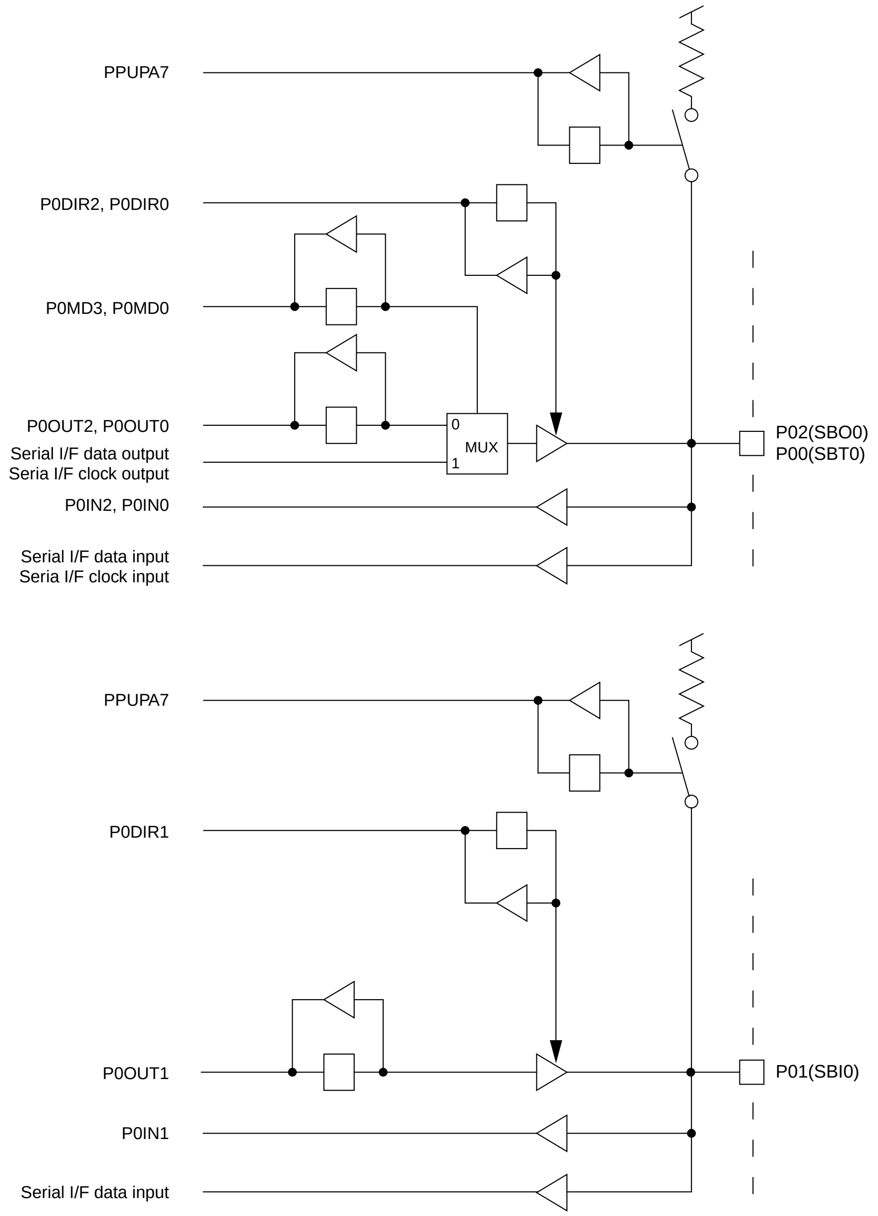
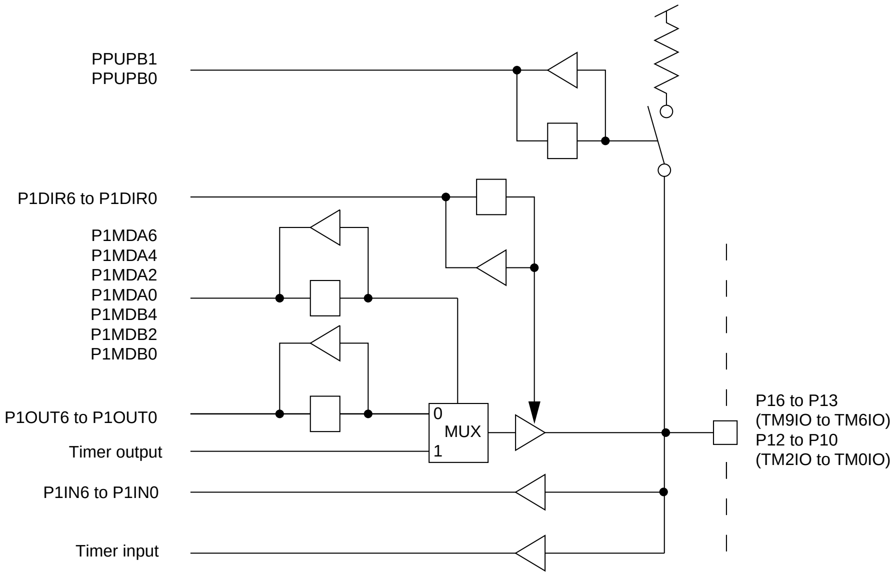
Port	Pin (Shared Pin)	Function
Port 0	P02 (SBO0) P01 (SBI0) P00 (SBT0)	Port 0 is used as the port 0 general-purpose port or the serial interface signal. At reset, this port operates as a general-purpose port input. (When this is used as a serial interface signal, multi-port selection register PMSEL should be set.) 

Table 7-1-1 Port Functions (2 of 7)

<table>
<tr><th>Port</th><th>Pin
(Shared Pin)</th><th>Function</th></tr>
<tr><td>Port 1</td><td>P16
(TM9IO)
P15
(TM8IO)
P14
(TM7IO)
P13
(TM6IO)
P12
(TM2IO)
P11
(TM1IO)
P10
(TM0IO)</td><td>Port 1 is used as the port 1 general-purpose port or timer I/O (TM9IO to TM6IO, TM2IO to TM0IO). At reset, this port operates as a general-purpose port input. (When this is used as TM7IO, TM6IO and TM2IO to TM0IO, multi-port selection register PMSEL should be set.)


</td></tr>
<tr><td>Port 2</td><td>P25 to P20
($\overline{IRQ5}$ to $\overline{IRQ0}$)</td><td>Port 2 is used as the port 2 general-purpose port or external interrupt signal. At reset, this port operates as a general-purpose port input. When $\overline{NMI}$ pin level is set to port input (P2IN6) to be readable, it is possible to detect malfunction by chattering with software.

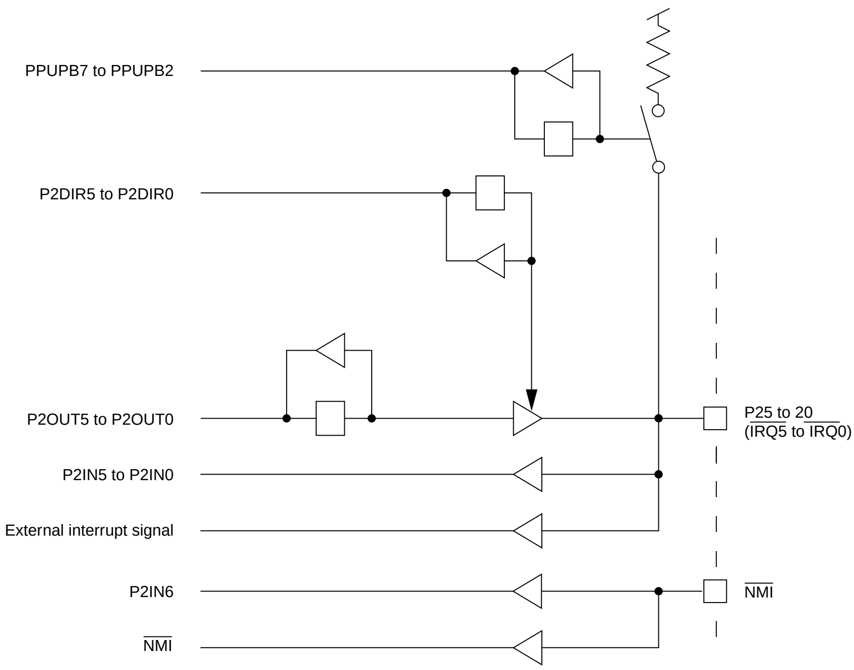

</td></tr>
</table>

Table 7-1-1 Port Functions (3 of 7)

Port	Pin (Shared Pin)	Function
Port 3	P37 to P30 (AN0 to AN7)	Port 3 is used as the port 3 general-purpose port or AD converter input. At reset, this port operates as a general-purpose port input. (When this is used as AD converter input, analog port selection register ANSEL should be set.)

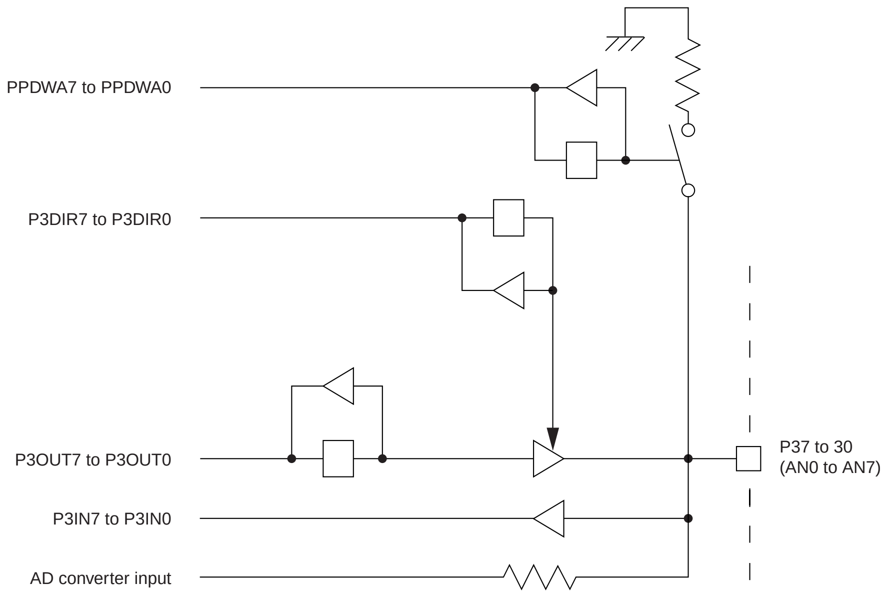


Table 7-1-1 Port Functions (4 of 7)

Port	Pin (Shared Pin)	Function
Port 4	P45 ($\overline{\text{PWM2}}$, STOP) P44 (PWM2, TM7IO) P43 ($\overline{\text{PWM1}}$, TM6IO) P42 (PWM1, TM2IO) P41 ($\overline{\text{PWM0}}$, TM1IO) P40 (PWM0, TM0IO)	Port 4 is used as the port 4 general-purpose port, 6-phase PWM output (TM11), timer I/O (TM7IO, TM6IO and TM2IO to TM0IO) or microcontroller status signal. At reset, this port operates as a general-purpose port input. (When this is used as TM7IO, TM6IO and TM2IO to TM0IO, multi-port selection register PMSEL should be set.)

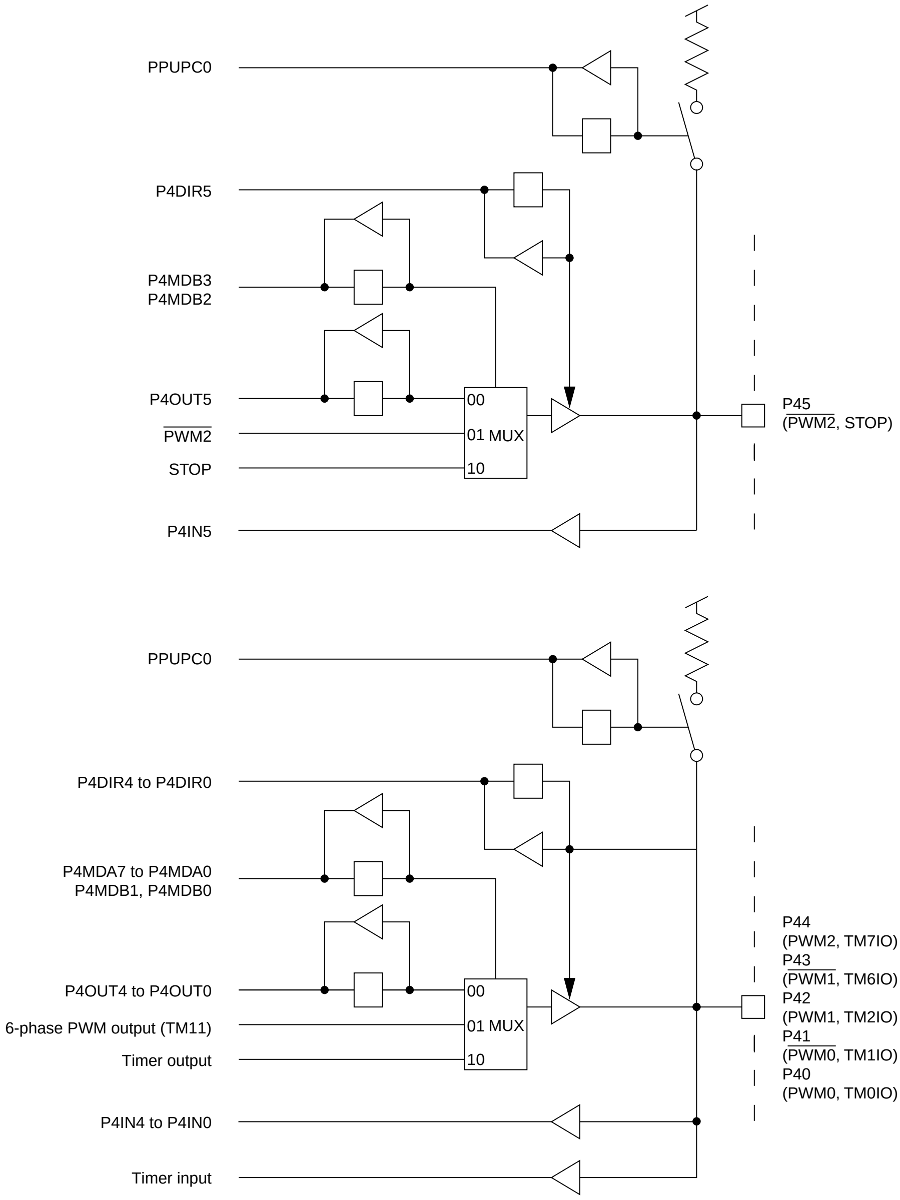


Table 7-1-1 Port Functions (5 of 7)

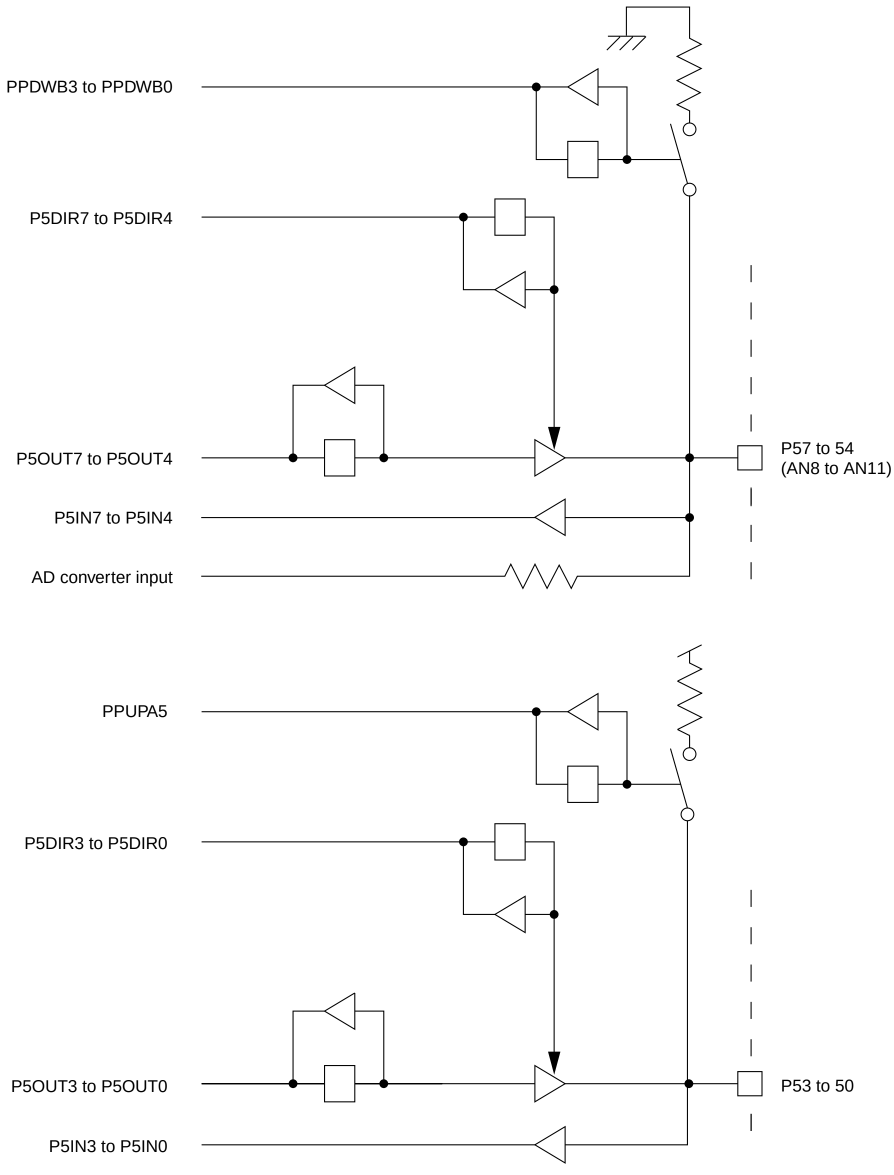
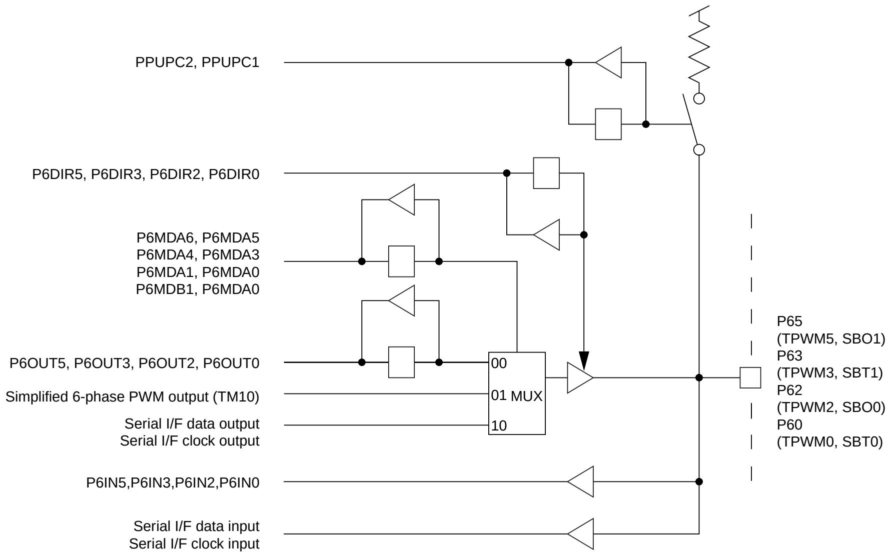
Port	Pin (Shared Pin)	Function
Port 5	P57 to P54 (AN8 to AN11) P53 to P50	Port 5 is used as the port 5 general-purpose port or AD converter input. At reset, this port operates as a general-purpose port input. (When this is used as AD converter, analog port selection register ANSEL and multi-port selection register PMSEL should be set.) 

Table 7-1-1 Port Functions (6 of 7)

Port	Pin (Shared Pin)	Function
Port 6	P65 (TPWM5, SBO1) P64 (TPWM4, SBI1) P63 (TPWM3, SBT1) P62 (TPWM2, SBO0) P61 (TPWM1, SBI0) P60 (TPWM0, SBT0)	Port 6 is used as the port 6 general-purpose port, simplified 6-phase PWM output or serial interface signal. At reset, this port operates as a general-purpose port input. (When this is used as serial interface signal ch0, multi-port selection register PMSEL should be set.)



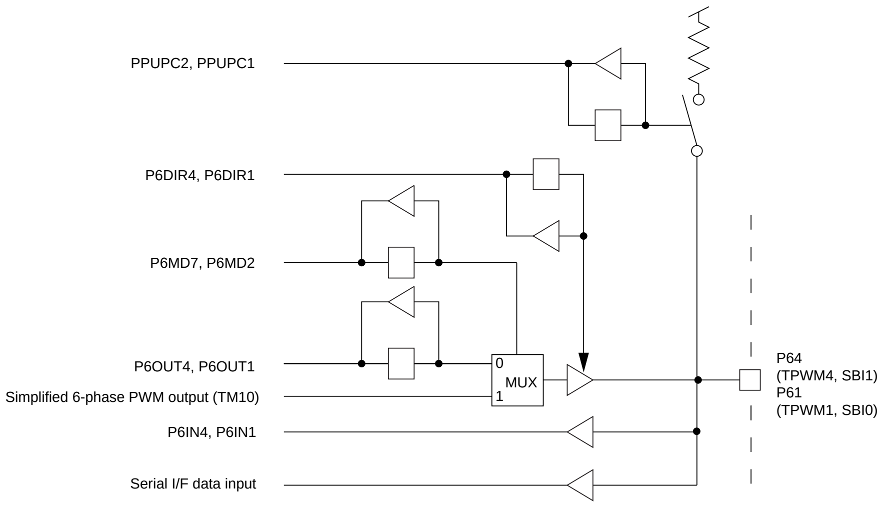
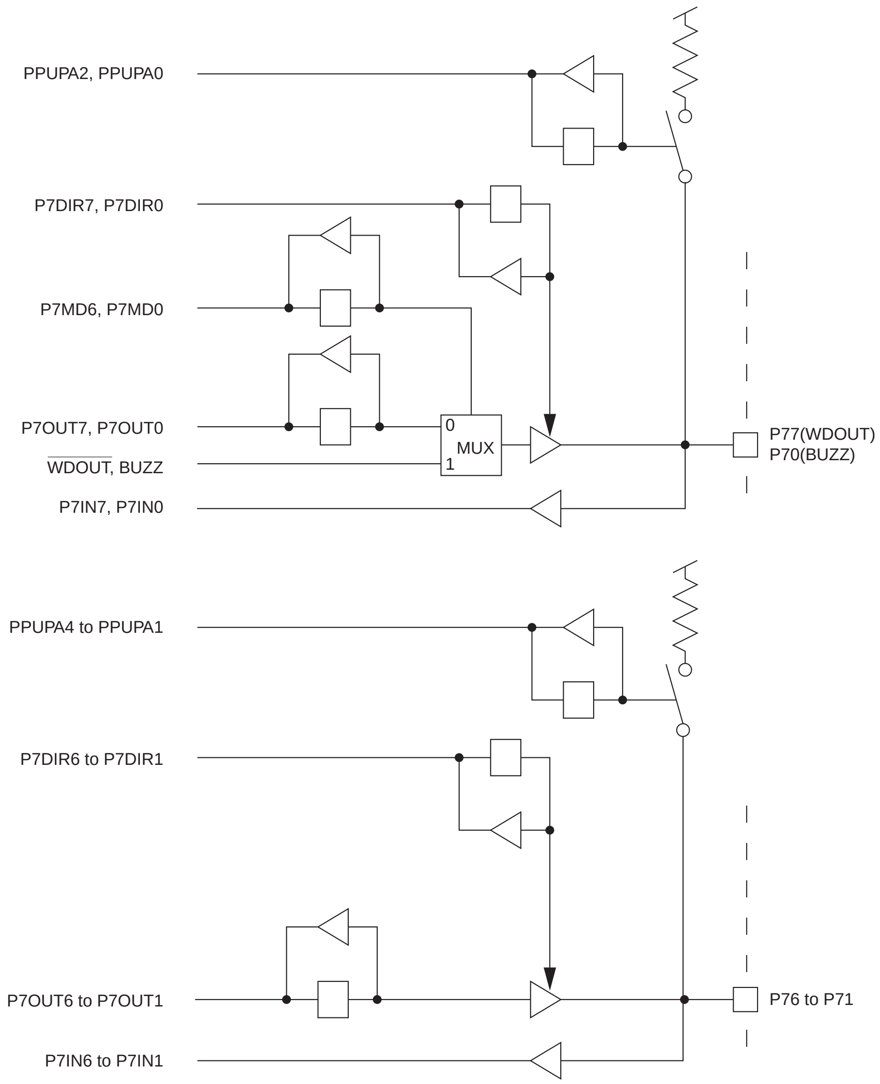


Table 7-1-1 Port Functions (7 of 7)

Port	Pin (Shared Pin)	Function
Port 7	P77 ($\overline{\text{WDOUT}}$) P76 to P71 P70 (BUZZ)	Port 7 is used as the port 7 general-purpose port, microcontroller status signal or buzzer output signal. At reset, this port operates as a general-purpose port input. 

7-1-2 Control Registers

This section describes the port control registers.

Table 7-1-2 List of Port Control Registers

Port0	Port0 output register	(P0OUT)	x'00FFC0'
	Port0 input register	(P0IN)	x'00FFD0'
	Port0 I/O control register	(P0DIR)	x'00FFE0'
	Port0 output mode register	(P0MD)	x'00FFF0'
Port1	Port1 output register	(P1OUT)	x'00FFC1'
	Port1 input register	(P1IN)	x'00FFD1'
	Port1 I/O control register	(P1DIR)	x'00FFE1'
	Port1 output mode register A	(P1MDA)	x'00FFF2'
	Port1 output mode register B	(P1MDB)	x'00FFF3'
Port2	Port2 output register	(P2OUT)	x'00FFC2'
	Port2 input register	(P2IN)	x'00FFD2'
	Port2 I/O control register	(P2DIR)	x'00FFE2'
Port3	Port3 output register	(P3OUT)	x'00FFC3'
	Port3 input register	(P3IN)	x'00FFD3'
	Port3 I/O control register	(P3DIR)	x'00FFE3'
	Port3 output mode register	(P3MD)	x'00FFF4'
Port4	Port4 output register	(P4OUT)	x'00FFC4'
	Port4 input register	(P4IN)	x'00FFD4'
	Port4 I/O control register	(P4DIR)	x'00FFE4'
	Port4 output mode register A	(P4MDA)	x'00FFF6'
	Port4 output mode register B	(P4MDB)	x'00FFF7'
Port5	Port5 output register	(P5OUT)	x'00FFC5'
	Port5 input register	(P5IN)	x'00FFD5'
	Port5 I/O control register	(P5DIR)	x'00FFE5'
	Port5 output mode register	(P5MD)	x'00FFF8'
Port6	Port6 output register	(P6OUT)	x'00FFC6'
	Port6 input register	(P6IN)	x'00FFD6'
	Port6 I/O control register	(P6DIR)	x'00FFE6'
	Port6 output mode register A	(P6MDA)	x'00FFFA'
	Port6 output mode register B	(P6MDB)	x'00FFFB'

Port7	Port7 output register Port7 input register Port7 I/O control register Port7 output mode register	(P7OUT) (P7IN) (P7DIR) (P7MD)	x'00FFC7' x'00FFD7' x'00FFE7' x'00FFFC'
Others	Multi-port selection register Analog port selection register Pull up control register A Pull up control register B Pull up control register C Pull down control register A Pull down control register B	(PMSEL) (ANSEL) (PPUPA) (PPUPB) (PPUPC) (PPDWA) (PPDWB)	x'00FFA0' x'00FFA2' x'00FFB0' x'00FFB1' x'00FFB2' x'00FFB4' x'00FFB5'

The port n output register (PnOUT) sets the data to be output. The port n input register (PnIN) reads the pin values. The port n input/output control register (PnDIR) sets the input or output of each bit. The port n output mode register (PnMD) selects the port output. The port pull-up control register (PPUP) sets pull-up of each pin. The port pull-down control register (PPDW) sets pull-down of each pin. The multi-port selection register (PMSEL) selects multi-port of serial interface, timer and analog. The analog port selection register (ANSEL) is selected in case of using a port as an analog pin.

Port setup is shown below.

■ P02 pin

Selection	P0DIR2	P0MD3	PMSEL2	Remarks
Port input	0	0	-	-
Serial input	0	1	0	At serial 2 channels
Port output	1	0	-	-
Serial output	1	1	0	-

■ P01 Pin

Selection	P0DIR1	PMSEL1
Port input	0	-
Serial input	0	0
Port output	1	-

■ P00 Pin

Selection	P0DIR0	P0MD0	PMSEL0
Port input	0	0	-
Serial clock input	0	1	0
Port output	1	0	-
Serial clock output	1	1	0

■ P16 Pin

Selection	P1DIR6	P1MDB4	Remarks
Port input	0	-	When pin input function is used on TM9, it is also operated as timer input pin.
TM9IO input			
Port output	1	0	-
TM9IO output	1	1	-

■ P15 Pin

Selection	P1DIR5	P1MDB2	Remarks
Port input	0	-	When pin input function is used on TM8, it is also operated as timer input pin.
TM8IO input			
Port output	1	0	-
TM8IO output	1	1	-

■ P14 Pin

Selection	P1DIR4	P1MDB0	PMSEL7
Port input	0	-	-
TM7IO input	0	-	0
Port output	1	0	-
TM7IO output	1	1	0

■ P13 Pin

Selection	P1DIR3	P1MDA6	PMSEL6
Port input	0	-	-
TM6IO input	0	-	0
Port output	1	0	-
TM6IO output	1	1	0

■ P12 Pin

Selection	P1DIR2	P1MDA4	PMSEL5
Port input	0	-	-
TM2IO input	0	-	0
Port output	1	0	-
TM2IO output	1	1	0

■ P11 Pin

Selection	P1DIR1	P1MDA2	PMSEL4
Port input	0	-	-
TM1IO input	0	-	0
Port output	1	0	-
TM1IO output	1	1	0

■ P10 Pin

Selection	P1DIR0	P1MDA0	PMSEL3
Port input	0	-	-
TM0IO input	0	-	0
Port output	1	0	-
TM0IO output	1	1	0

■ P25 to P20 Pins

<table>
<tr><th>Selection</th><th>P2DIRn
(n=5 to 0)</th></tr>
<tr><td>Port input</td><td rowspan="2">0</td></tr>
<tr><td>Interrupt input</td></tr>
<tr><td>Port output</td><td>1</td></tr>
</table>

■ P37 to P30 Pins

Selection	P3DIRn (n=7 to 0)	ANSELn (n=7 to 0)	PMSELn (n=11 to 8)	Remarks
Port input	0	0	-	-
Analog input (AN0 to AN7)	0	1	0	When AN4 to AN7 are used, set PMSEL.
Port output	1	-	-	-

■ P45 Pin

Selection	P4DIR5	P4MDB3	P4MDB2
Port input	0	-	-
Port output	1	0	0
$\overline{\text{PWM2}}$ output	1	0	1
STOP	1	1	0

■ P44 Pin

Selection	P4DIR4	P4MDB1	P4MDB0	PMSEL7
Port input	0	-	-	-
TM7IO input	0	-	-	1
Port output	1	0	0	-
PWM2 output	1	0	1	-
TM7IO output	1	1	0	1

■ P43 Pin

Selection	P4DIR3	P4MDA7	P4MDA6	PMSEL6
Port input	0	-	-	-
TM6IO input	0	-	-	1
Port output	1	0	0	-
$\overline{\text{PWM1}}$ output	1	0	1	-
TM6IO output	1	1	0	1

■ P42 Pin

Selection	P4DIR2	P4MDA5	P4MDA4	PMSEL5
Port input	0	-	-	-
TM2IO input	0	-	-	1
Port output	1	0	0	-
PWM1 output	1	0	1	-
TM2IO output	1	1	0	1

■ P41 Pin

Selection	P4DIR1	P4MDA3	P4MDA2	PMSEL4
Port input	0	-	-	-
TM1IO input	0	-	-	1
Port output	1	0	0	-
PWM0 output	1	0	1	-
TM1IO output	1	1	0	1

■ P40 Pin

Selection	P4DIR0	P4MDA1	P4MDA0	PMSEL3	Remarks
Port input	0	-	-	-	-
TM0IO input	0	-	-	1	-
Port output	1	0	0	-	-
PWM0 output	1	-	1	-	When P4MDA1 is 1, PWM output is inhibited at NMI generation.
TM0IO output	1	1	0	1	-

■ P57 to P54 Pins

Selection	P5DIRn (n=7 to 4)	ANSELn (n=11 to 8)	PMSELn (n=11 to 8)
Port input	0	0	-
Analog input (AN8 to AN11)	0	1	1
Port output	1	-	-

■ P53 to P50 Pins

Selection	P5DIRn (n=3 to 0)
Port input	0
Port output	1

■ P65 Pin

Selection	P6DIR5	P6MDB1	P6MDB0	Remarks
Port input	0	0	0	-
Serial input	0	1	0	At serial 2 channels
Port output	1	0	0	-
TPWM5 output	1	0	1	-
Serial output	1	1	0	-

■ P64 Pin

Selection	P6DIR4	P6MDA7
Port input	0	-
Serial input	0	-
Port output	1	0
TPWM4 output	1	1

■ P63 Pin

Selection	P6DIR3	P6MDA6	P6MDA5
Port input	0	0	0
Serial clock input	0	1	0
Port output	1	0	0
TPWM3 output	1	0	1
Serial clock output	1	1	0

■ P62 Pin

Selection	P6DIR2	P6MDA4	P6MDA3	PMSEL2	Remarks
Port input	0	0	0	-	-
Serial input	0	1	0	1	At serial 2 channels
Port output	1	0	0	-	-
TPWM2 output	1	0	1	-	-
Serial output	1	1	0	1	-

■ P61 Pin

Selection	P6DIR1	P6MDA2	PMSEL1
Port input	0	-	-
Serial input	0	-	1
Port output	1	0	-
TPWM1 output	1	1	-

■ P60 Pin

Selection	P6DIR0	P6MDA1	P6MDA0	PMSEL0
Port input	0	0	0	-
Serial clock input	0	1	0	1
Port output	1	0	0	-
TPWM0 output	1	0	1	-
Serial clock output	1	1	0	1

■ P77 Pin

Selection	P7DIR7	P7MD6
Port input	0	-
Port output	1	0
$\overline{\text{WDOUT}}$ output	1	1

■ P76 to P71 Pins

Selection	P7DIRn (n=6 to 1)
Port input	0
Port output	1

■ P70 Pin

Selection	P7DIR0	P7MD0
Port input	0	-
Port output	1	0
BUZZ output	1	1

7-2 Pull-up/Pull-down Control Register

7-2-1 Overview

This LSI series contains a pin which sets a pull-up/pull-down resistor using the program.

Table 7-2-1 Pull-up/Pull-down Control Register

Pull up				Pull down			
Register	Bit	Relative pin number	Remarks	Regsiter	Bit	Relative pin number	Remarkes
PPUPA	7	33 to 35	P02 to P00	PPDWA	7	32	P37
	6	reserved	Set always to '0'.		6	31	P36
	5	17 to 20	P53 to P50		5	30	P35
	4	7	P76		4	29	P34
	3	6	P75		3	28	P33
	2	3 to 5, 8	P77, P74 to P72		2	27	P32
	1	2	P71		1	26	P31
	0	1	P70		0	25	P30
PPUPB	7	48	P25	PPDWB	7	-	-
	6	47	P24		6	-	-
	5	46	P23		5	-	-
	4	45	P22		4	-	-
	3	44	P21		3	24	P57
	2	43	P20		2	23	P56
	1	41, 42	P16, P15		1	22	P55
	0	36 to 40	P14 to P10		0	21	P54
PPUPC	7	-	-				
	6	-	-				
	5	-	-				
	4	-	-				
	3	reserved	Set always to '0'.				
	2	58 to 60	P65 to P63				
	1	55 to 57	P62 to P60				
	0	49 to 54	P45 to P40				

Chapter 8 Appendices

8

8-1 Electrical Characteristics

8-1-1 Electrical Characteristics

This LSI manual describes about standard specification.
Before using this manual, please obtain product specifications from the sales office.

Structure	CMOS integrated circuit
Application	General purpose
Function	16-bit microcontroller
Pin Configuration	Figure 1-4-1
Package Dimension	Figure 1-5-1

A. Absolute Maximum Ratings

V_{SS} = 0 V

Parameter		Symbol	Rating	Unit
A1	Power supply voltage	V_{DD}	-0.3 to +7.0	V
A2	Input pin voltage	V_I	-0.3 to V_{DD}+0.3	V
A3	output pin voltage	V_O	-0.3 to V_{DD}+0.3	V
A4	Input /output pin voltage	V_{IO}	-0.3 to V_{DD}+0.3	V
A5	Operating ambient temperature	Topr	-20 to +70	°C
A6	Storage temperature	Tstg	-55 to +125	°C

Notes)

(1) Absolute Maximum Ratings are stress ratings not to cause damage to the device. Operation at these ratings is not guaranteed.

(2) All of the V_{DD} and V_{SS} pins are external pins. Connect them directly to the power source and ground.

(3) To prevent latch-up tolerance, connect more than one bypass condenser between power supply pins and ground. Use a condenser of 0.2 µF or more.

B. Operating Conditions

V_{SS} = 0 V
Ta = -20 °C to +70 °C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
B1	Power supply voltage	V_{DD1}	$F_{osc1} \le 5$ MHz	4.5		5.5	V
B2	Power supply voltage	V_{DD2}	$F_{osc1} = 4$ MHz	3.9		5.5	V
Crystal Oscillator 1 (OSCI)							
B3	Oscillator frequency	F_{osc1}	V_{DD} = 4.5 V to 5.5 V			5	MHz

C. Electrical Characteristics

(1) DC Characteristics

V_{DD} = 5.0 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
C1	Power supply current during operation	I_{DD1}	V_I = V_{DD} or V_{SS} F_{OSC1} = 5 MHz Output pins open			75	mA
C2	Power supply current in STOP mode	I_{DD2}	Oscillator stop All functions stop			50	µA
C3	Power supply current in HALT0 mode	I_{DD3}	F_{OSC1} = 5 MHz			30	mA

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Input/Output Pins 1 <Output push pull/input CMOS level schmitt trigger /with programmable pull up>: P74 to P77							
C4	Input high voltage	V_{IH1}		V_{DD}×0.8			V
C5	Input low voltage	V_{IL1}				V_{DD}×0.2	V
C6	Output high voltage	V_{OH1}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C7	Output low voltage	V_{OL1}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C8	Output leakage current	I_{LO1}	V_O = Hi-Z			±10	µA
C9	Pull-up resistor	R_{PU1}	V_{DD} = 5.0 V V_I = 0.0 V	12	30	75	kΩ
Input/Output Pins 2 <Output push pull/input CMOS level schmitt trigger /with programmable pull up>: P15, P16, P20 to P25, P40 to P45, P60 to P65, P70 to P73							
C10	Input high voltage	V_{IH2}		V_{DD}×0.8			V
C11	Input low voltage	V_{IL2}				V_{DD}×0.2	V
C12	Output high voltage	V_{OH2}	V_{DD} = 5.0 V I_{OH} = -2.0 mA	V_{DD}-0.6			V
C13	Output low voltage	V_{OL2}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C14	Output leakage current	I_{LO2}	V_O = Hi-Z			±10	µA
C15	Pull-up resistor	R_{PU2}	V_{DD} = 5.0 V V_I = 0.0 V	12	30	75	kΩ

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Input/Output Pins 3 <Output push pull/input CMOS level/with programmable pull up>: P00 to P02, P10 to P14, P50 to P52							
C16	Input high voltage	V_{IH3}		$V_{DD}\times0.8$			V
C17	Input low voltage	V_{IL3}				$V_{DD}\times0.2$	V
C18	Output high voltage	V_{OH3}	V_{DD} = 5.0 V I_{OH} = -2.0 mA	V_{DD}-0.6			V
C19	Output low voltage	V_{OL3}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C20	Output leakage current	I_{LO3}	V_O = Hi-Z			±10	µA
C21	Pull-up resistor	R_{PU3}	V_{DD} = 5.0 V V_I = 0.0 V	12	30	75	kΩ
Input/Output Pins 4 <Output push pull/input TTL level/analog input/with programmable pull down>: P30 to P37, P53 to P57							
C22	Input high voltage	V_{IH4}		2.4			V
C23	Input low voltage	V_{IL4}				0.8	V
C24	Output high voltage	V_{OH4}	V_{DD} = 5.0 V I_{OH} = -2.0 mA	V_{DD}-0.6			V
C25	Output low voltage	V_{OL4}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C26	Output leakage current	I_{LO4}	V_O = Hi-Z			±10	µA
C27	Pull-down resistor	R_{PU1}	V_{DD} = 5.0 V V_I = 5.0 V	8	20	50	kΩ
Input Pin 1 <Input CMOS level schmitt/with pull up>: /RST							
C28	Input high voltage	V_{IH5}		$V_{DD}\times0.9$			V
C29	Input low voltage	V_{IL5}				$V_{DD}\times0.1$	V
C30	Pull-up resistor	R_{PU4}	V_{DD} = 5.0 V V_I = 0.0 V	12	30	75	kΩ

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Output Pin <Output push pull>: SYSCLK							
C31	Output high voltage	V_{OH5}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C32	Output low voltage	V_{OL5}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
Input Pin 2 <Input CMOS level schmitt>: /NMI							
C33	Input high voltage	V_{IH6}		V_{DD}×0.9			V
C34	Input low voltage	V_{IL6}				V_{DD}×0.1	V
C35	Input leakage current	I_{LO5}	V_{DD} = 5.5 V V_I = V_{SS} to V_{DD}			±10	µA
OSCI pin (at external clock input): in case of self-excited oscillation by crystal or ceramic							
C36	Input high voltage	V_{IH7}		V_{DD}×0.8		V_{DD}	V
C37	Input low voltage	V_{IL7}		V_{SS}		V_{DD}×0.2	V
Pin capacitance							
C38	Input pin	C_{IN}	V_{IN} = 0 V Ta = 25 °C		7	15	pF
C39	Output pin	C_{OUT}			7	15	pF
C40	Input/output pin	$C_{I/O}$			7	15	pF

D. A/D Converter Characteristics

V_{DD} = 5.0 V
V_{SS} = 0 V
Ta = 25 °C

<table>
<tr><th colspan="2" rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2" rowspan="2">Conditions</th><th colspan="3">Capacitance</th><th rowspan="2">Unit</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>D1</td><td>Resolution</td><td></td><td colspan="2"></td><td></td><td></td><td>10</td><td>Bits</td></tr>
<tr><td rowspan="2">D2</td><td rowspan="2">Power supply current in STOP mode</td><td rowspan="2"></td><td rowspan="2">V_{DD} = 5 V
V_{SS} = 0 V</td><td>AN3 to 0</td><td></td><td></td><td>±3</td><td>LSB</td></tr>
<tr><td>AN11 to 4</td><td></td><td></td><td>±4</td><td>LSB</td></tr>
<tr><td>D3</td><td>A/D Conversion Time</td><td></td><td colspan="2">Fosc=5 MHz</td><td>11.2</td><td></td><td></td><td>µs</td></tr>
<tr><td>D4</td><td>Analog input voltage</td><td>V_{IA}</td><td colspan="2"></td><td>V_{SS}</td><td></td><td>V_{DD}</td><td>V</td></tr>
</table>

E. AC Characteristics (Input)

Input Timing Conditions

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
External Clock Input Timing (Fosc1 = 5 MHz)							
E1	External clock input cycle time	t_{EXCcyc}	Fig 8-1	200			ns
E2	External clock input high pulse width	t_{EXCH}		$\frac{t_{EXCcyc}}{2}$ -5			ns
E3	External clock input low pulse width	t_{EXCL}		$\frac{t_{EXCcyc}}{2}$ -5			ns
E4	External clock input rising time	t_{EXCR}				5	ns
E5	External clock input falling time	t_{EXCF}				5	ns
Reset input timing							
E6	Reset signal pulse width (/RST)	t_{RSTW}	Fig 8-2	1			t_{EXCcyc}

Input Timing Conditions

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Interrupt signal input timing							
E7	Non-maskable interrupt signal pulse width (NMI)	t_{NMIW}	Fig 8-3	5 (Note1)			t_{cyc}
E8	External interrupt signal pulse width (/IRQ5 to 0)	t_{IRQW}		2 (Noter2)			t_{cyc}

(Note1) When sampling cycle of noise filter is 't_{cyc}', even if the noise of the specified time or less is input, an interrupt may occur.
(Note2) When sampling cycle of noise filter is 't_{cyc}', even if the noise of the specified time or less is input, an interrupt may occur.
It is when the noise filter of /IRQ3 to 0 is disabled.

Input Timing Conditions

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Serial Interface Related Signal Timing (Synchronous Serial Reception)							
E9	Reception data setup time (SBI1 to 0)	t_{RXDS}	Fig 8-5	25			ns
E10	Reception data hold time (SBI1 to 0)	t_{RXDH}		25			ns
E11	Serial clock input high pulse width (SBT1 to 0)	t_{SCH}		t_{cyc}+100			ns
E12	Serial clock input low pulse width (SBT1 to 0)	t_{SCL}		t_{cyc}+100			ns
Timer/Counter signal input timing							
E13	Timer external inptu clock low pulse width (TMnIO:n = 9 to 6 and 2 to 0)	t_{TCCLKL}	Fig 8-6	t_{cyc}			ns
E14	Timer external input clock high pulse width (TMnIO:n = 9 to 6 and 2 to 0)	t_{TCCLKH}		t_{cyc}			ns

F. AC Characteristics (Output)

Output Signal Characteristics

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C
C_L = 70 pF

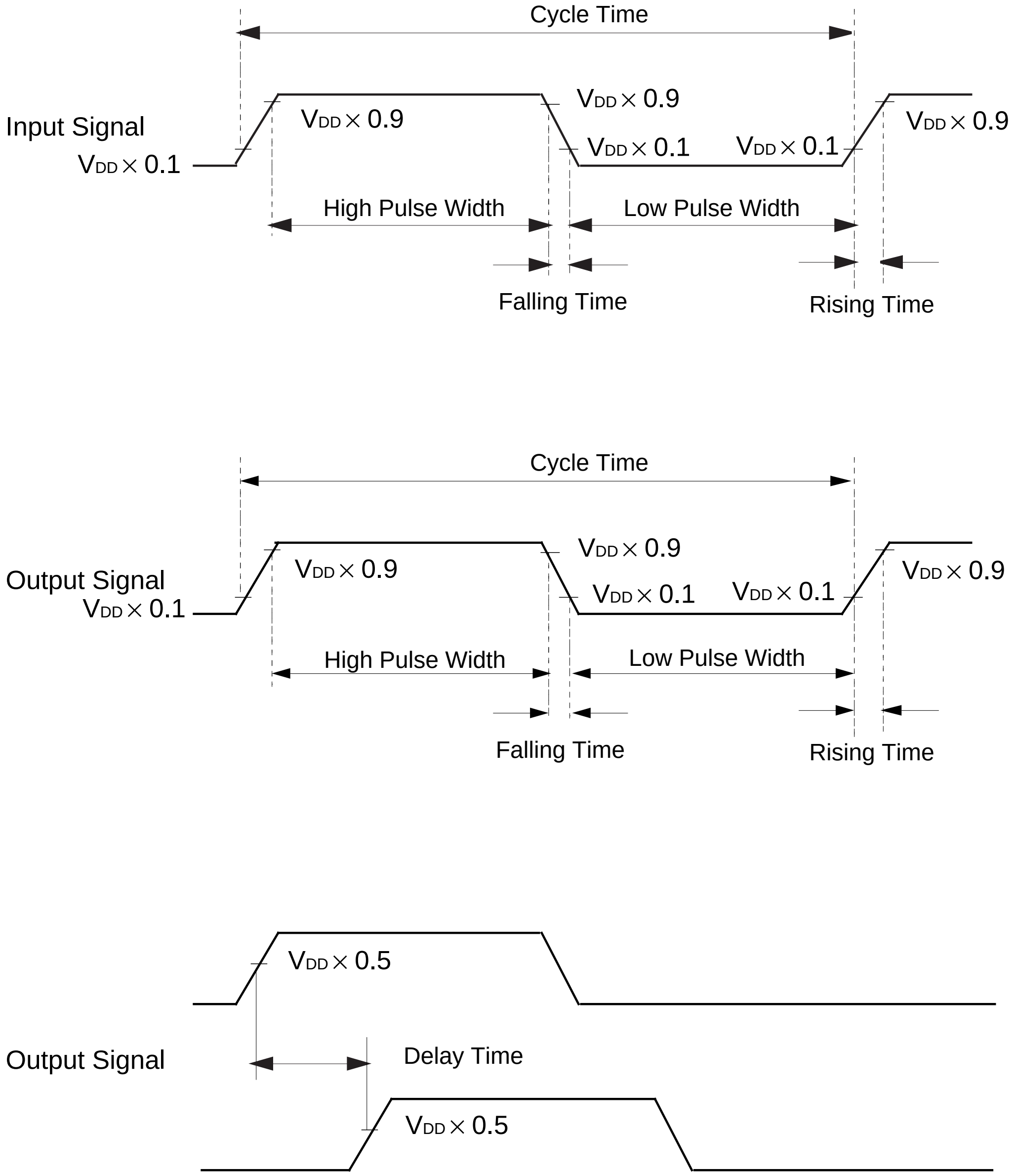
Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
System Clock Output Timing							
F1	System clock output cycle time (SYSCLK)	t_{cyc}	Fig 8-1	100			ns
F2	System clock output low pulse width (SYSCLK)	t_{CL}		45			ns
F3	System clock output high pulse width (SYSCLK)	t_{CH}		35			ns
F4	Sytem clock output rising time (SYSCLK)	t_{CR}				10	ns
F5	System clock outptu falling time (SYSCLK)	t_{CF}				10	ns

Output Signal Characteristics

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -20 °C to +70 °C
C_L = 70 pF

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Serial Interface Signal Output Timing 1 (at Synchronous Serial Transmission)							
F6	Transfer data delay time (SBO1 to 0)	t_{TXDD}	Fig 8-4			$\frac{t_{cyc}}{2}$	ns
F7	Transfer data hold time (transfer in progress) (SBO1 to 0)	t_{TXDH1}	Fig 8-4	10			ns

AC Timing Voltage Level



(Both setup time and hold time are $V_{DD} \times 0.5$)

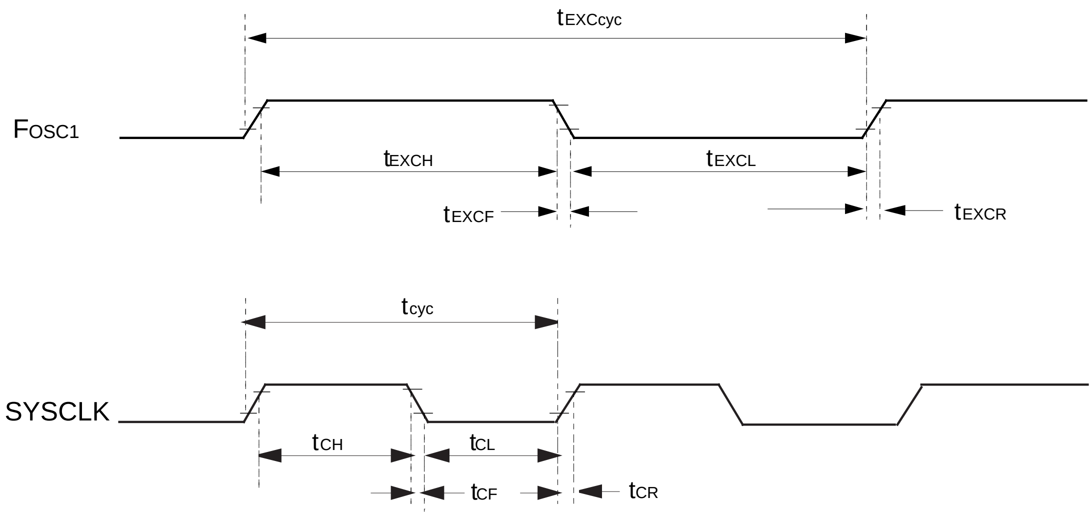


Figure 8-1 System Clock Timing

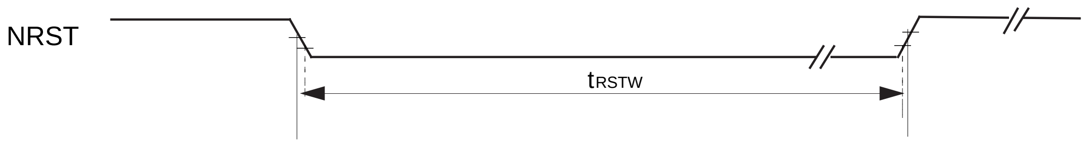


Figure 8-2 Reset Timing

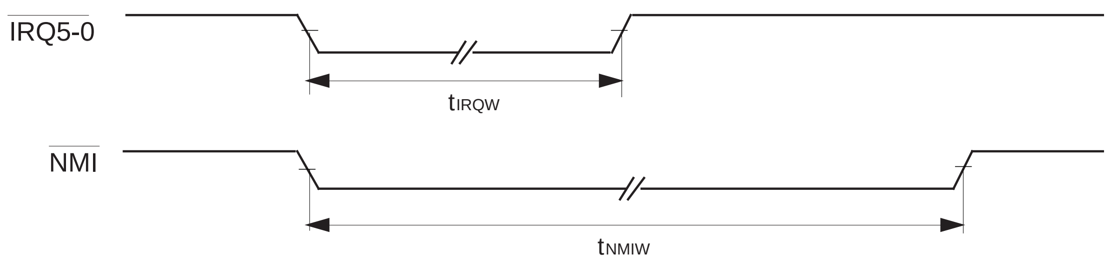


Figure 8-3 Interrupt Signal Timing

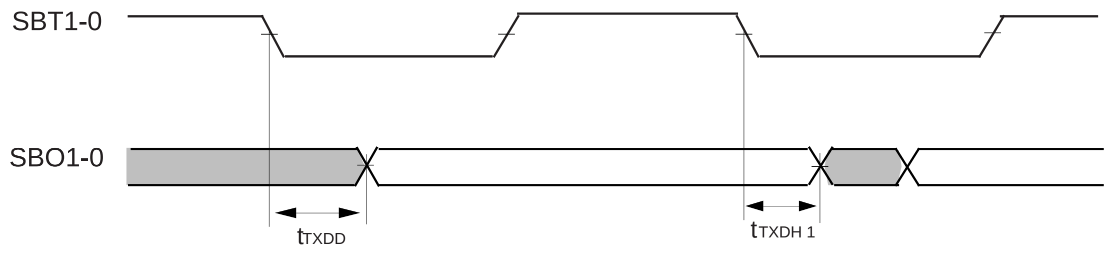


Figure 8-4 Serial Interface Signal Timing 1
(At Synchronous Serial Interface Falling Edge Transmission: Timing during Transfer)

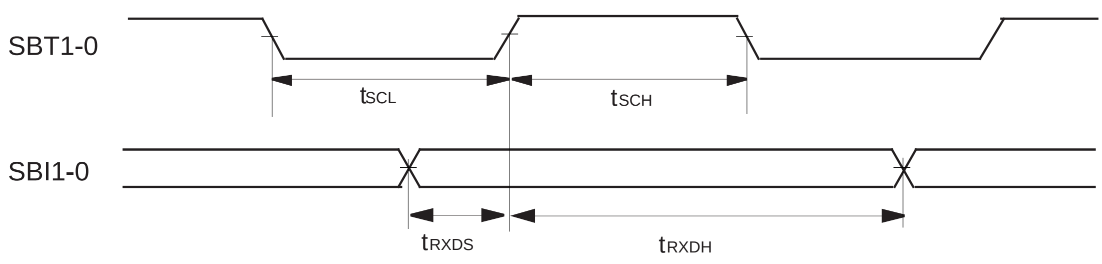


Figure 8-5 Serial Interface Signal Timing 2
(At Synchronous Serial Interface Rising Edge Reception)

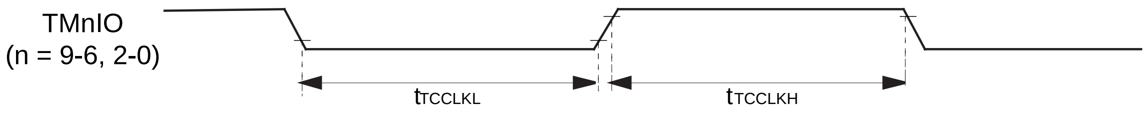


Figure 8-6 Timer Counter Signal Timing

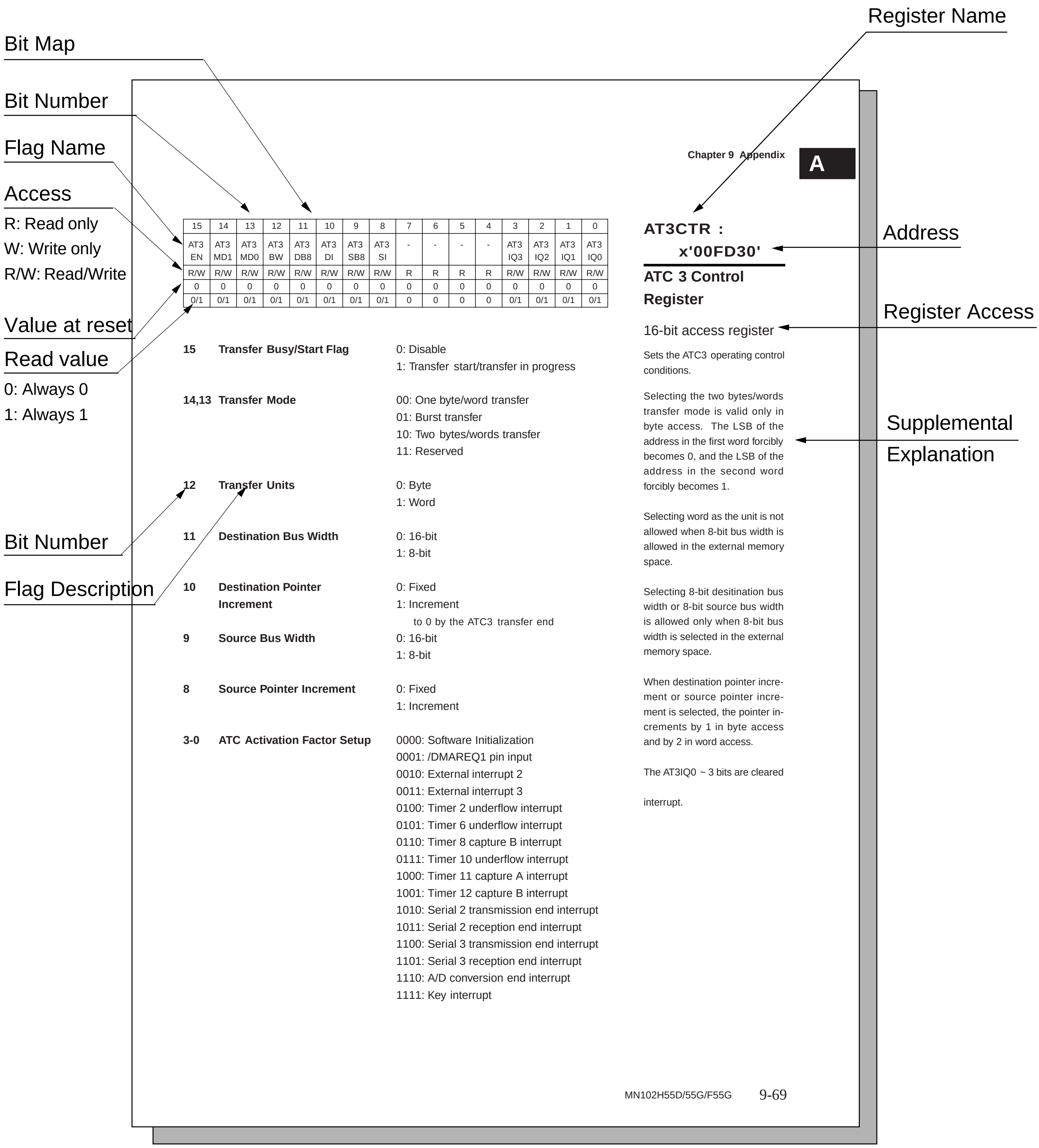
8-2 Data Appendices

8-2-1 Special Function Registers

About This Section

■ Description of Each Page

Each page of this chapter describes one or more registers. Each page lists the register name, address, register access, bit map, flag explanation of each bit number and supplementary explanation. The following is the layout and definition of this section.



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AT3 EN	AT3 MD1	AT3 MD0	AT3 BW	AT3 DB8	AT3 DI	AT3 SB8	AT3 SI	-	-	-	-	AT3 IQ3	AT3 IQ2	AT3 IQ1	AT3 IQ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0/1	0/1	0/1	0/1

AT3CTR :
x'00FD30'

ATC 3 Control Register

16-bit access register

15	**Transfer Busy/Start Flag**	0: Disable 1: Transfer start/transfer in progress
14,13	**Transfer Mode**	00: One byte/word transfer 01: Burst transfer 10: Two bytes/words transfer 11: Reserved
12	**Transfer Units**	0: Byte 1: Word
11	**Destination Bus Width**	0: 16-bit 1: 8-bit
10	**Destination Pointer Increment**	0: Fixed 1: Increment to 0 by the ATC3 transfer end
9	**Source Bus Width**	0: 16-bit 1: 8-bit
8	**Source Pointer Increment**	0: Fixed 1: Increment
3-0	**ATC Activation Factor Setup**	0000: Software Initialization 0001: /DMAREQ1 pin input 0010: External interrupt 2 0011: External interrupt 3 0100: Timer 2 underflow interrupt 0101: Timer 6 underflow interrupt 0110: Timer 8 capture B interrupt 0111: Timer 10 underflow interrupt 1000: Timer 11 capture A interrupt 1001: Timer 12 capture B interrupt 1010: Serial 2 transmission end interrupt 1011: Serial 2 reception end interrupt 1100: Serial 3 transmission end interrupt 1101: Serial 3 reception end interrupt 1110: A/D conversion end interrupt 1111: Key interrupt

Sets the ATC3 operating control conditions.

Selecting the two bytes/words transfer mode is valid only in byte access. The LSB of the address in the first word forcibly becomes 0, and the LSB of the address in the second word forcibly becomes 1.

Selecting word as the unit is not allowed when 8-bit bus width is allowed in the external memory space.

Selecting 8-bit desitination bus width or 8-bit source bus width is allowed only when 8-bit bus width is selected in the external memory space.

When destination pointer increment or source pointer increment is selected, the pointer increments by 1 in byte access and by 2 in word access.

The AT3IQ0 ~ 3 bits are cleared

interrupt.

MN102H55D/55G/F55G   9-69

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD RST	WD 1ng1	WD 1ng0	-	-	-	-	-	-	-	-	OSC ID	STOP	HALT	OSC1	OSC0
R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
1	0	0	0	0	1	1	1	0	0	1	1	0	1	1	1
0/1	0/1	0/1	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1

C

CPUM : x'00FC00'

CPU Mode Control Register

16-bit access register

15 Watchdog Timer Enable
0: Enable
1: Disable and clear (at reset)

Setting WDRST to '0' after setting it to '1' clears the watchdog timer counting value and starts counting.
The watchdog timer consists of a 17-bit binary counter counting on the oscillation clock. Therefore, clear the watchdog timer counting value within 2^{16} (65,536) machine cycles.

14:13 Watchdog Timer Count
00: 2^{16}
01: 2^{4}
10: 2^{8}
11: Reserved

Changing the set value shortens the stabilization wait time when returning from STOP mode. (At reset release, the stabilization wait time is fixed to 2^{16} (65,536) machine cycles.

4 System Clock Monitor
0: High-speed 1: Low-speed

3 CPU Operating Control (STOP transfer request)

2 CPU Operating Control (HALT transfer request)

1:0 Oscillator Control

0000: NORMAL mode
0001: IDLE mode
0011: Reserved
0100: HALT0 mode
0111: Reserved
1000: STOP0 mode
1011: Reserved

The following describes programming rules and precautions in the STOP/HALT mode.

Points for Programming

(1) After setting the CPUM address in the address register in advance, use the register indirect addressing mode for the MOV instruction of the CPUM register setup.
(2) Immediately after the MOV instruction, locate three NOPs consecutively.
(3) Immediately before the MOV instruction, locate the JMP instruction and align to the even address. This avoids the effects by the differences of the bus widths in the memory mode or expansion mode, and provides the same result when operating in any conditions.

Programming Coding Example in Assembler (as 102 Ver.1.0, Ver.2.0)

```
          MOV    CPUM, A0   ;  Set the CPUM address to A0.
          MOV    (A0), D0   ;  Transfer the contents of CPUM to D0.
          OR     x'000*', D0 ;  Generate the data to set the STOP/HALT mode.
          JMP    STP_HLT    ;  Branch unconditionally to the even address  to
          ALIGN  2              eliminate the difference of operating conditions.
STP_HLT   MOV    D0, (A0)   ;  Set CPUM to the STOP/HALT mode.
          NOP               ;  Dummy
          NOP               ;  Dummy
          NOP               ;  Dummy
```

Precautions

(1) * of OR instruction varies depending on the STOP mode or HALT mode.
(2) Set the ALIGN value to '2' or more in the file that describes the above examples when the ALIGN value is set using SECTION dummy instruction before this programming coding described. If the ALIGN value is set to '1', an error occurs in the line of the ALIGN instruction .
(3) Code the above programming in the assembler source file of another file when the program is developed with C complier cc 102.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	HSWT IOE	NWAI TIOE	WAIT SET	ARBSZ	-	WAIT IO1	WAIT IO0	-	WAIT2	WAIT1	WAIT0
R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	1	1	1	0	0	1	1	0	1	1	1
0	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0	0/1	0/1	0/1

MEMCTR : x'00FC02'

Memory Control Register

16-bit access register

In this LSI register series, set MEMCTR to x'0410' or x'0490'.

10 Peripheral Fixed Wait Cycle Enable Flag During Handshake Mode
0: No Wait
1: Peripheral Fixed Wait Cycle
(Always set '1' in this series.)

9 Peripheral Fixed Wait Cycle Enable Flag
0: Enable 1: Disable
(Always set '0' in this series.)

8 Fixed Wait Mode/ Handshake Mode Switch
0: Handshake Mode
1: Fixed Wait Mode
(Always set '0' in this series.)

7 Bus Width Setup Flag for Fixed Area (x'040000' to x'07FFFF')
0: Based on $\overline{\text{WORD}}$ pin
1: 8-bit Bus Access regardless of $\overline{\text{WORD}}$ pin

5:4 Peripheral Fixed Wait Cycle
00: No wait
01: 1 wait cycle
10: 2 wait cycles
11: 3 wait cycles
(Always set '01' in this series.)

2:0 Fixed Wait Cycle
000: No wait cycle
001: 1 wait cycle
010: 2 wait cycles
011: 3 wait cycles
100: 4 wait cycles
101: 5 wait cycles
110: 6 wait cycles
111: 7 wait cycles
(Don't care in this series.)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	GN4	GN3	GN2	GN1	GN0	-
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0

IAGR : x'00FC0E'

Interrupt Accept Group Register

8/16-bit access register

IAGR is a read-only register.

5:1 Group Number of Accepted Interrupt

I

M

7	6	5	4	3	2	1	0
SYS C7	SYS C6	SYS C5	SYS C4	SYS C3	SYS C2	SYS C1	SYS C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	1	1	1	1	0	1
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SYSCTL : x'00FC32'

System Control Register

8-bit access register

Not rewrite registers related system.

7:0 Inhibitation of Rewriting Registers Related System

7D: All registers can be rewritten.
Except for 7D: Registers below are inhibited to rewrite.

Internal control	CPUM
Memory control	MEMMD
	EXMCTR
Port control	P0MD
	P1MDA, P1MDB
	P3MD
	P4MDA, P4MDB
	P5MD
	P6MDA, P6MDB
	P7MD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	UNIF	WDIF	NMIF
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

G0ICR : x'00FC40'

Non-maskable interrupt control register 0

8/16-bit access register

2 **Non-maskable Interrupt Request Flag by Executing an Undefined Instruction**
0: No interrupt requested
1: Interrupt requested

1 **Non-maskable Interrupt Request Flag by Overflow of Watchdog Timer**
0: No interrupt requested
1: Interrupt requested

0 **Non-maskable Interrupt Request Flag by $\overline{\text{NMI}}$ Pin**
0: No interrupt requested
1: Interrupt requested

G

S

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G1 LV2	G1 LV1	G1 LV0	TM0 IE	IRQ2 IE	IRQ1 IE	IRQ0 IE	TM0 IR	IRQ2 IR	IRQ1 IR	IRQ0 IR	TM0 ID	IRQ2 ID	IRQ1 ID	IRQ0 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

G1ICR : x'00FC42'

Maskable Interrupt Control Register 1

8/16-bit access register

14:12 Group 1 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

11 Timer 0 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

10 IRQ2 Interrupt Enable Flag — 0: Disable 1: Enable

9 IRQ1 Interrupt Enable Flag — 0: Disable 1: Enable

8 IRQ0 Interrupt Enable Flag — 0: Disable 1: Enable

7 Timer 0 Underflow Interrupt Request Flag — 0: No interrupt requested
1: Interrupt requested

6 IRQ2 Interrupt Request Flag — 0: No interrupt requested
1: Interrupt requested

5 IRQ1 Interrupt Request Flag — 0: No interrupt requested
1: Interrupt requested

4 IRQ0 Interrupt Request Flag — 0: No interrupt detected
1: Interrupt detected

3 Timer 0 Underflow Interrupt Detect Flag — 0: No interrupt detected
1: Interrupt detected

2 IRQ2 Interrupt Detection Flag — 0: No interrupt detected
1: Interrupt detected

1 IRQ1 Interrupt Detection Flag — 0: No interrupt detected
1: Interrupt detected

0 IRQ0 Interrupt Detection Flag — 0: No interrupt detected
1: Interrupt detected

'1' is set when timer 0 underflows.
'1' is set when an external interrupt occurs from IRQ0 pin.
'1' is set when an external interrupt occurs from IRQ1 pin.
'1' is set when an external interrupt occurs from IRQ2 pin.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G2 LV2	G2 LV1	G2 LV0	AN IE	IRQ5 IE	IRQ4 IE	IRQ3 IE	AN IR	IRQ5 IR	IRQ4 IR	IRQ3 IR	AN ID	IRQ5 ID	IRQ4 ID	IRQ3 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

G2ICR : x'00FC44'

Maskable Interrupt Control Register 2

8/16-bit access register

G

14:12 Group 2 Interrupt Priority Level 000 (level 0) to 110 (level 6)

11 A/D Conversion End Interrupt Enable Flag 0: Disable 1: Enable

10 IRQ5 Interrupt Enable Flag 0: Disable 1: Enable

9 IRQ4 Interrupt Enable Flag 0: Disable 1: Enable

8 IRQ3 Interrupt Enable Flag 0: Disable 1: Enable

7 A/D Conversion End Interrupt Request Flag
0: No interrupt requested
1: Interrupt requested

6 IRQ5 Interrupt Request Flag
0: No interrupt requested
1: Interrupt requested

5 IRQ4 Interrupt Request Flag
0: No interrupt requested
1: Interrupt requested

4 IRQ3 Interrupt Request Flag
0: No interrupt requested
1: Interrupt requested

3 A/D Conversion End Interrupt Detection Flag
0: No interrupt detected
1: Interrupt detected

2 IRQ5 Interrupt Detection Flag
0: No interrupt detected
1: Interrupt detected

1 IRQ4 Interrupt Detection Flag
0: No interrupt detected
1: Interrupt detected

0 IRQ3 Interrupt Detection Flag
0: No interrupt detected
1: Interrupt detected

'1' is set when the A/D conversion ends.
'1' is set when an external interrupt occurs from IRQ3 pin.
'1' is set when an external interrupt occurs from IRQ4 pin.
'1' is set when an external interrupt occurs from IRQ5 pin.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G3 LV2	G3 LV1	G3 LV0	-	SC0 IE	TM2 IE	TM1 IE	-	SC0 IR	TM2 IR	TM1 IR	-	SC0 ID	TM2 ID	TM1 ID
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1

G3ICR : x'00FC46'

Maskable Interrupt Control Register 3

8/16-bit access register

14:12 Group 3 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

10 Serial Interface 0 Transmission End Interrupt Enable Flag — 0: Disable 1: Enable

9 Timer 2 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 Timer 1 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

6 Serial Interface 0 Transmission End Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

5 Timer 2 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

4 Timer 1 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

'1' is set when the serial 0 reception ends.
'1' is set when timer 2 underflows.
'1' is set when timer 1 underflows.

2 Serial Interface 0 Transmission End Interrupt Detection Flag — 0: No interrupt detected 1: Interrupt detected

1 Timer 2 Underflow Interrupt Detection Flag — 0: No interrupt detected 1: Interrupt detected

0 Timer 1 Underflow Interrupt Detection Flag — 0: No interrupt detected 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G4 LV2	G4 LV1	G4 LV0	-	SC1 IE	TM8 IE	TM3 IE	-	SC1 IR	TM8 IR	TM3 IR	-	SC1 ID	TM8 ID	TM3 ID
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1

G4ICR : x'00FC48'

Maskable Interrupt Control Register 4

8/16-bit access register

G

14:12 Group 4 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

10 Serial Interface 1 Transmission End Interrupt Enable Flag — 0: Disable 1: Enable

9 Timer 8 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 Timer 3 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

6 Serial Interface 1 Transmission End Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

5 Timer 8 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

4 Timer 3 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

'1' is set when the serial 1 reception ends.
'1' is set when timer 8 underflows.
'1' is set when timer 3 underflows.

2 Serial Interface 1 Transmission End Interrupt Detection Flag — 0: No interrupt detected 1: Interrupt detected

1 Timer 8 Underflow Interrupt Detection Flag — 0: No interrupt detected 1: Interrupt detected

0 Timer 3 Underflow Interrupt Detection Flag — 0: No interrupt detected 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G5 LV2	G5 LV1	G5 LV0	-	TM9 IE	TM5 IE	TM4 IE	-	TM9 IR	TM5 IR	TM4 IR	-	TM9 ID	TM5 ID	TM4 ID
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1

G5ICR : x'00FC4A'

Maskable Interrupt Control Register 5

8/16-bit access register

14:12 Group 5 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

10 Timer 9 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

9 Timer 5 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 Timer 4 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

6 Timer 9 Underflow Interrupt Request Flag — 0: No interrupt requested; 1: Interrupt requested

'1' is set when timer 9 underflows.

5 Timer 5 Underflow Interrupt Request Flag — 0: No interrupt requested; 1: Interrupt requested

'1' is set when timer 5 underflows.

4 Timer 4 Underflow Interrupt Request Flag — 0: No interrupt requested; 1: Interrupt requested

'1' is set when timer 4 underflows.

2 Timer 9 Underflow Interrupt Detection Flag — 0: No interrupt detected; 1: Interrupt detected

1 Timer 5 Underflow Interrupt Detection Flag — 0: No interrupt detected; 1: Interrupt detected

0 Timer 4 Underflow Interrupt Detection Flag — 0: No interrupt detected; 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G6 LV2	G6 LV1	G6 LV0	-	-	TM6 IE	TM10 IE	-	-	TM6 IR	TM10 IR	-	-	TM6 ID	TM10 ID
R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1

G6ICR : x'00FC4C'

Maskable Interrupt Control Register 6

8/16-bit access register

G

14:12 Group 6 Interrupt Priority Level 000 (level 0) to 110 (level 6)

9 Timer 6 Underflow Interrupt Enable Flag 0: Disable 1: Enable

9 Timer 10 Overflow Interrupt Enable Flag 0: Disable 1: Enable

5 Timer 6 Underflow Interrupt Request Flag 0: No interrupt requested
1: Interrupt requested

'1' is set when timer 6 underflows.

4 Timer 10 Overflow Interrupt Request Flag 0: No interrupt requested
1: Interrupt requested

'1' is set when timer 10 overflows.

1 Timer 6 Underflow Interrupt Detection Flag 0: No interrupt detected
1: Interrupt detected

0 Timer 10 Overflow Interrupt Detection Flag 0: No interrupt detected
1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G7 LV2	G7 LV1	G7 LV0	*Note	*Note	TM7 IE	TM11 IE	*Note	*Note	TM7 IR	TM11 IR	-	-	TM7 ID	TM11 ID
R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1

* Note) Set always '0'.

G7ICR : x'00FC4E'

Maskable Interrupt Control Register 7

8/16-bit access register

14:12 Group 7 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

9 Timer 7 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 Timer 11 Under/Overflow Interrupt Enable Flag — 0: Disable 1: Enable

5 Timer 7 Underflow Interrupt Request Flag — 0: No interrupt requested; 1: Interrupt requested

4 Timer 11 Under/Overflow Interrupt Request Flag — 0: No interrupt requested; 1: Interrupt requested

'1' is set when timer 7 underflows.
'1' is set when timer 11 under/overflows.

1 Timer 7 Underflow Interrupt Detection Flag — 0: No interrupt detected; 1: Interrupt detected

0 Timer 11 Under/Overflow Interrupt Detection Flag — 0: No interrupt detected; 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	IRQ5 TG1	IRQ5 TG0	IRQ4 TG1	IRQ4 TG0	IRQ3 TG1	IRQ3 TG0	IRQ2 TG1	IRQ2 TG0	IRQ1 TG1	IRQ1 TG0	IRQ0 TG1	IRQ0 TG0
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

EXTMD : x'00FC50'

External Interrupt Edge Setup Register

8/16-bit access register

E

G

11:10 IRQ 5 Pin Interrupt Conditions
00: Low level
01: High level
10: Negative (falling) edge
11: Positive (rising) edge

9:8 IRQ 4 Pin Interrupt Conditions
00: Low level
01: High level
10: Negative (falling) edge
11: Positive (rising) edge

When this is used at STOP, "L" level or "R" level should be set. At STOP, edge interrupt is not available. (Even if edge is set, interrupt occurs by level.)

7:6 IRQ 3 Pin Interrupt Conditions
00: Low level
01: High level
10: Negative (falling) edge
11: Positive (rising) edge

5:4 IRQ 2 Pin Interrupt Conditions
00: Low level
01: High level
10: Negative (falling) edge
11: Positive (rising) edge

3:2 IRQ 1 Pin Interrupt Conditions
00: Low level
01: High level
10: Negative (falling) edge
11: Positive (rising) edge

1:0 IRQ 0 Pin Interrupt Conditions
00: Low level
01: High level
10: Negative (falling) edge
11: Positive (rising) edge

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	IRQ3 FSE	IRQ3 FEN	IRQ2 FSE	IRQ2 FEN	IRQ1 FSE	IRQ1 FEN	IRQ0 FSE	IRQ0 FEN	NMI SEL1	NMI SEL0
R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

NFCTR : x'00FC52'

Interrupt Noise Filter Control Register

8/16-bit access register

9 IRQ 3 Noise Filter Sampling Cycle
0: 2^2 machine cycles
1: 2^7 machine cycles

8 IRQ 3 Noise Filter Enable
0: OFF 1: ON

When noise filter enable is ON, waveform input from interrupt pin is sampled. This is sent to within CPU when "L" level more than sampling 4 cycles is input.

7 IRQ 2 Noise Filter Sampling Cycle
0: 2^2 machine cycles
1: 2^7 machine cycles

6 IRQ 2 Noise Filter Enable
0: OFF 1: ON

5 IRQ 1 Noise Filter Sampling Cycle
0: 2^2 machine cycles
1: 2^7 machine cycles

4 IRQ 1 Noise Filter Enable
0: OFF 1: ON

3 IRQ 0 Noise Filter Sampling Cycle
0: 2^2 machine cycles
1: 2^7 machine cycles

2 IRQ 0 Noise Filter Enable
0: OFF 1: ON

1:0 NMI Noise Filter Sampling Cycle
00: 1 machine cycle
01: 2^2 machine cycles
10: 2^7 machine cycles
11: Inhibited

Noise filter of NMI pin is always operating. This is sent to within CPU when "L" level more than sampling 5 cycles is input.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD CLR	-	-	-	-	-	WD P1	WD P0	-	-	-	-	-	BZEN	BZP1	BZP0
R/W	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0	0	0	0	0	0/1	0/1	0	0	0	0	0	0/1	0/1	0/1

WDREG : x'00FC54'

Watchdog Expansion and Buzzer Output Control Register

16-bit access register

15 Clear the Expansion Watchdog Counter

0: Not clear/enable
1: Clear/disable

Extend the watchdog interrupt occurrence period set by CPUM register.

9:8 Watchdog Interrupt Occurrence Period

00: Watchdog period set by CPUM register × 1
01: Watchdog period set by CPUM register × 8
10: Watchdog period set by CPUM register × 16
11: Watchdog period set by CPUM register × 32

In this period, count is done by expansion watchdog counter.

When the counter value of watchdog is cleared, be sure to clear the 15th bit of CPUM. At expansion, the 15th bit of WDREG also should be cleared.

Before selecting expansion period *× 8, × 16, × 32 of WDREG, set always WDCLR of WDREG15 to '1'.*

2 Buzzer Output Permission

0: Disable
1: Enable

1:0 Buzzer Output Frequency Selection

00: $1/2^{15}$ of system clock
01: $1/2^{14}$ of system clock
10: $1/2^{13}$ of system clock
11: $1/2^{12}$ of system clock

N

W

7	6	5	4	3	2	1	0
SC0 CE1	SC0 CE0	-	SC0 DIR	SC0 STE	SC0 LNG2	SC0 LNG1	SC0 LNG0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1
0/1	0/1	0	0/1	0/1	0/1	0/1	0/1

SC0MD0 : x'00FD80'

Serial 0 Mode Register 0

8/16-bit access register

7:6 Transfer Timing Selection

Transfer data output edge	Reception data input edge
00: Falling	Rising
01: Falling	Falling
10: Rising	Falling
11: Rising	Rising

4 Deliver Bit Order

0: From MSB 1: From LSB

3 Synchronous Serial Start Condition Selection

0: Disabled 1: Enabled

2:0 Synchronous Serial Transfer Bit Count

000: 1 bit
001: 2 bits
010: 3 bits
011: 4 bits
100: 5 bits
101: 6 bits
110: 7 bits
111: 8 bits

SC0MD1 : x'00FD81'

Serial 0 Mode Register 1

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
SC0 IOM	-	SC0 SBIS	-	SC0 CKM	SC0 MST	-	SC0 CMD
R/W	R	R/W	R	R/W	R/W	R	R/W
0	0	0	0	0	0	0	0
0/1	0	0/1	0	0/1	0/1	0	0/1

7 Serial Data Input Selection
0: Serial input from SBI0 (RXD0)
1: Serial Input from SBO0 (TXD0)

5 Serial Input Control
0: 1 input 1: Serial input

3 1/8 Division Selection of Transfer Clock
0: Not divide 1: divide

2 Clock Master Slave Selection
0: Clock slave
1: Clock master

0 Transfer Mode Setup
0: Synchronous 1: Half-duplex UART

S

7	6	5	4	3	2	1	0
SC0 FM1	SC0 FM0	SC0 PM1	SC0 PM0	SC0 NPE	-	SC0 BRKF	SC0 BRKE
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0	0/1	0/1

SC0MD2 : x'00FD82'

Serial 0 Mode Register 2

8/16-bit access register

7:6 Flame Mode Specification
00: Data 7 bits × Stop 1 bit
01: Data 7 bits × Stop 2 bits
10: Data 8 bits × Stop 1 bit
11: Data 8 bits × Stop 2 bits

5:4 Parity Additional Bit Specification
00: 0
01: 1
10: Even
11: Odd

3 Parity Enable
0: Enable 1: Disable

1 Break Status Reception Monitor
0: Data reception
1: Break reception

0 Break Status Deliver Control
0: Data transmission
1: Break transmission

7	6	5	4	3	2	1	0
SC0 BSY	-	SC0 TEMP	SC0 REMP	SC0 FEF	SC0 PEK	SC0 ORE	SC0 ERE
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0	0/1	0/1	0/1	0/1	0/1	0/1

SC0MD3 : x'00FD83'

Serial 0 Mode Register 3

8-bit access register
(16-bit access is possible from even address.)

7 Serial Bus Use Status
0: Except during serial transfer
1: During serial transfer

5 Transmission Buffer Empty Flag
0: Transmission buffer empty
1: Transmission buffer full

4 Reception Buffer Empty Flag
0: Reception buffer empty
1: Reception buffer full

3 Flaming Error Detection
0: Error does not occur.
1: Error occurs.

2 Parity Error Detection
0: Error does not occur.
1: Error occurs.

1 Overrun Error Detection
0: Error does not occur.
1: Error occurs.

0 Error Monitor Flag
0: Error does not occur.
1: Error occurs.

S

7	6	5	4	3	2	1	0
-	-	-	SC0 TNF	SC0 ODC1	SC0 ODC0	SC0 CS1	SC0 CS0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0/1	0/1	0/1	0/1

SC0CKS : x'00FD84'

Serial 0 Clock Source Control Register

8/16-bit access register

4 SBT0 Noise Filter Control
0: OFF
1: ON

3 SBO0 Nch Open-drain Control
0: OFF
1: ON

2 SBT0 Nch Open-drain Control
0: OFF
1: ON

If Nch open-drain control is ON, be sure to select SBT0 output or SBO0 output by port output mode register.

1:0 Clock Source Selection
00: 2 dividing of system clock
01: 4 dividing of system clock
10: 16 dividing of system clock
11: 2 dividing of TM3 output clock

At clock slave, select a clock witch is not beyond external clock.

RXBUF0 : x'00FD86'

Serial 0 Reception Buffer

8/16-bit access register

7	6	5	4	3	2	1	0
RX BUF07	RX BUF06	RX BUF05	RX BUF04	RX BUF03	RX BUF02	RX BUF01	RX BUF00
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Serial Reception Data

TXBUF0 : x'00FD87'

Serial 0 Transmission Buffer

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
TX BUF07	TX BUF06	TX BUF05	TX BUF04	TX BUF03	TX BUF02	TX BUF01	TX BUF00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Serial Transmission Data

7	6	5	4	3	2	1	0
SC1 CE1	SC1 CE0	-	SC1 DIR	SC1 STE	SC1 LNG2	SC1 LNG1	SC1 LNG0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1
0/1	0/1	0	0/1	0/1	0/1	0/1	0/1

SC1MD0 : x'00FD90'

Serial 1 Mode Register 0

8/16-bit access register

7:6 Transfer Timing Selection

Transfer data output edge	Reception data input edge
00: Falling	Rising
01: Falling	Falling
10: Rising	Falling
11: Rising	Rising

4 Deliver Bit Order

0: From MSB 1: From LSB

3 Synchronous Serial Start Condition Selection

0: Disabled 1: Enabled

2:0 Synchronous Serial Transfer Bit Count

000: 1 bit
001: 2 bits
010: 3 bits
011: 4 bits
100: 5 bits
101: 6 bits
110: 7 bits
111: 8 bits

SC1MD1 : x'00FD91'

Serial 1 Mode Register 1

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
SC1 IOM	-	SC1 SBIS	-	SC1 CKM	SC1 MST	-	SC1 CMD
R/W	R	R/W	R	R/W	R/W	R	R/W
0	0	0	0	0	0	0	0
0/1	0	0/1	0	0/1	0/1	0	0/1

7	**Serial Data Input Selection**	0: Serial input from SBI1 (RXD1) 1: Serial input from SBO1 (TXD1)	
5	**Serial Input Control**	0: 1 input	1: Serial input
3	**1/8 Dividing Selection of Transfer Clock**	0: Not divided	1: Divided
2	**Clock Master Slave Selection**	0: Clock slave 1: Clock master	
0	**Transfer Mode Setup**	0: Synchronous	1: Half-duplex UART

S

7	6	5	4	3	2	1	0
SC1 FM1	SC1 FM0	SC1 PM1	SC1 PM0	SC1 NPE	-	SC1 BRKF	SC1 BRKE
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0	0/1	0/1

SC1MD2 : x'00FD92'

Serial 1 Mode Register 2

8/16-bit access register

7:6 Flame Mode Specification

00: Data 7 bits × Stop 1 bit
01: Data 7 bits × Stop 2 bits
10: Data 8 bits × Stop 1 bit
11: Data 8 bits × Stop 2 bits

5:4 Parity Additional Bit Specification

00: 0
01: 1
10: Odd
11: Even

3 Parity Enable

0: Enable 1: Disable

1 Break Status Reception Monitor

0: Data reception
1: Break reception

0 Break Status Deliver Control

0: Data transmission
1: Break transmission

7	6	5	4	3	2	1	0
SC1 BSY	-	SC1 TEMP	SC1 REMP	SC1 FEF	SC1 PEK	SC1 ORE	SC1 ERE
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0	0/1	0/1	0/1	0/1	0/1	0/1

SC1MD3 : x'00FD93'

Serial 1 Mode Register 3

8-bit access register
(16-bit access is possible from even address.)

7 Serial Bus Use Status
0: Except during serial transfer
1: During serial transfer

5 Transfer Buffer Empty Flag
0: Transmission buffer empty
1: Transmission buffer full

4 Reception Buffer Empty Flag
0: Reception buffer empty
1: Reception buffer full

3 Flaming Error Detection
0: Error does not occur.
1: Error occurs.

2 Parity Error Detection
0: Error does not occur.
1: Error occurs.

1 Overrun Error Detection
0: Error does not occur.
1: Error occurs.

0 Error Monitor Flag
0: Error does not occur.
1: Error occurs.

S

7	6	5	4	3	2	1	0
-	-	-	SC1 TNF	SC1 ODC1	SC1 ODC0	SC1 CS1	SC1 CS0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0/1	0/1	0/1	0/1

SC1CKS : x'00FD94'

Serial 1 Clock Source Control Register

8/16-bit access register

4 **SBT1 Noise Filter Control**
0: OFF
1: ON

3 **SBO1 Nch Open-drain Control**
0: OFF
1: ON

If Nch open-drain control is ON, be sure to select SBT1 output or SBO1 output by port output mode register.

2 **SBT1 Nch Open-drain Control**
0: OFF
1: ON

1:0 **Clock Source Selection**
00: 2 dividing of system clock
01: 4 dividing of system clock
10: 16 dividing of system clock
11: 2 dividing of TM3 output clock

At clock slave, select a clock witch is not beyond external clock .

RXBUF1 : x'00FD96'

Serial 1 Reception Buffer

8/16-bit access register

7	6	5	4	3	2	1	0
RX BUF17	RX BUF16	RX BUF15	RX BUF14	RX BUF13	RX BUF12	RX BUF11	RX BUF10
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Serial Reception Data

TXBUF1 : x'00FD97'

Serial 1 Transmission Buffer

8/16-bit access register
(16-bit access is possible
from even address.)

7	6	5	4	3	2	1	0
TX BUF17	TX BUF16	TX BUF15	TX BUF14	TX BUF13	TX BUF12	TX BUF11	TX BUF10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Serial Transmission Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	AN NCH2	AN NCH1	AN NCH0	-	AN ICH2	AN ICH1	AN ICH0	AN EN	AN ST1	AN ST0	AN CK2	AN CK1	AN CK0	AN MD1	AN MD0
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

ANCTR : x'00FDB0'

AD Conversion Control Register

8/16-bit access register

14:12 Ch Number at Multi-channels Conversion

000: ch0
001: ch0, 1
010: ch0, 1, 2
011: ch0, 1, 2, 3
100: ch0, 1, 2, 3, 4
101: ch0, 1, 2, 3, 4, 5
110: ch0, 1, 2, 3, 4, 5, 6
111: ch0, 1, 2, 3, 4, 5, 6, 7

Multi port selection register PMSEL selects AN4 to AN7 or AN8 to AN11 to connect it to ch 4 to ch7.

10:8 Ch Number at a Channel Conversion

000 (ch0) to 111 (ch7)

7 Conversion Start and Execution Flag

0: Inhibited
1: Conversion starts or during conversion

6:5 Conversion Start Selection

00: Start by conversion start and execution flag
01: Start by conversion start and execution flag
10: Start by underflow of TM1
11: Start by PWMST of TM11

4:2 Clock

000: SYSCLK
001: 2 dividing of SYSCLK
010: 4 dividing of SYSCLK
011: 8 dividing of SYSCLK
100: 16 dividing of SYSCLK
101: reserved
110: reserved
111: reserved

At 2.5 MHz to 5 MHz oscillation, 011 and 100 are possible. At 1.25 MHz to 2.5 MHz oscillation, 010, 011 and 100 are possible.

1:0 Operation Mode

00: 1 ch, 1 conversion
01: Multi-channels, 1 conversion for each
10: 1 ch, continuous conversion
11: Multi-channels, continuous conversion

AN0BUF : x'00FDC0'

AN0 Conversion Data Buffer

16-bit access register

AN0BUF is a read-only register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	AN0 BUF9	AN0 BUF8	AN0 BUF7	AN0 BUF6	AN0 BUF5	AN0 BUF4	AN0 BUF3	AN0 BUF2	AN0 BUF1	AN0 BUF0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9:0 A/D Conversion Result of ch0 (AN0 pin)

AN1BUF : x'00FDC2'

AN1 Conversion Data Buffer

16-bit access register

AN1BUF is a read-only register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	AN1 BUF9	AN1 BUF8	AN1 BUF7	AN1 BUF6	AN1 BUF5	AN1 BUF4	AN1 BUF3	AN1 BUF2	AN1 BUF1	AN1 BUF0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9:0 A/D Conversion Result of ch1 (AN1 pin)

AN2BUF : x'00FDC4'

AN2 Conversion Data Buffer

16-bit access register

AN2BUF is a read-only register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	AN2 BUF9	AN2 BUF8	AN2 BUF7	AN2 BUF6	AN2 BUF5	AN2 BUF4	AN2 BUF3	AN2 BUF2	AN2 BUF1	AN2 BUF0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9:0 A/D Conversion Result of ch2 (AN2 pin)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	AN3 BUF9	AN3 BUF8	AN3 BUF7	AN3 BUF6	AN3 BUF5	AN3 BUF4	AN3 BUF3	AN3 BUF2	AN3 BUF1	AN3 BUF0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

AN3BUF : x'00FDC6'

AN3 Conversion Data Buffer

16-bit access register

AN3BUF is a read-only register.

9:0 A/D Conversion Result of ch3 (AN3 pin)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	AN4 BUF9	AN4 BUF8	AN4 BUF7	AN4 BUF6	AN4 BUF5	AN4 BUF4	AN4 BUF3	AN4 BUF2	AN4 BUF1	AN4 BUF0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

AN4BUF : x'00FDC8'

AN4 Conversion Data Buffer

16-bit access register

AN4BUF is a read-only register.

9:0 A/D Conversion Result of ch4 (AN4 pin and AN8 pin)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	AN5 BUF9	AN5 BUF8	AN5 BUF7	AN5 BUF6	AN5 BUF5	AN5 BUF4	AN5 BUF3	AN5 BUF2	AN5 BUF1	AN5 BUF0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

AN5BUF : x'00FDCA'

AN5 Conversion Data Buffer

16-bit access register

AN5BUF is a read-only register.

9:0 A/D Conversion Result of ch2 (AN5 pin and AN9 pin)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	AN6 BUF9	AN6 BUF8	AN6 BUF7	AN6 BUF6	AN6 BUF5	AN6 BUF4	AN6 BUF3	AN6 BUF2	AN6 BUF1	AN6 BUF0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

AN6BUF : x'00FDCC'

AN6 Conversion Data Buffer

16-bit access register

AN6BUF is a read-only register.

9:0 A/D Conversion Result of ch6 (AN6 pin and AN10 pin)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	AN7 BUF9	AN7 BUF8	AN7 BUF7	AN7 BUF6	AN7 BUF5	AN7 BUF4	AN7 BUF3	AN7 BUF2	AN7 BUF1	AN7 BUF0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

AN7BUF : x'00FDCE'

AN7 Conversion Data Buffer

16-bit access register

AN7BUF is a read-only register.

9:0 A/D Conversion Result of ch7 (AN7 pin and AN11 pin)

TM0BC : x'00FE00'

Timer 0 Binary Counter

8/16-bit access register

TM0BC is a read-only register.

7	6	5	4	3	2	1	0
TM0 BC7	TM0 BC6	TM0 BC5	TM0 BC4	TM0 BC3	TM0 BC2	TM0 BC1	TM0 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Counter Value of Timer 0

TM1BC : x'00FE01'

Timer 1 Binary Counter

8/16-bit access register

TM1BC is a read-only register.

7	6	5	4	3	2	1	0
TM1 BC7	TM1 BC6	TM1 BC5	TM1 BC4	TM1 BC3	TM1 BC2	TM1 BC1	TM1 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Counter Value of Timer 1

TM2BC : x'00FE02'

Timer 2 Binary Counter

8/16-bit access register

TM2BC is a read-only register.

7	6	5	4	3	2	1	0
TM2 BC7	TM2 BC6	TM2 BC5	TM2 BC4	TM2 BC3	TM2 BC2	TM2 BC1	TM2 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Counter Value of Timer 2

TM3BC : x'00FE03'

Timer 3 Binary Counter

8-bit access register (16-bit access is possible from even address.)

TM3BC is a read-only register.

7	6	5	4	3	2	1	0
TM3 BC7	TM3 BC6	TM3 BC5	TM3 BC4	TM3 BC3	TM3 BC2	TM3 BC1	TM3 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Counter Value of Timer 3

TM4BC : x'00FE04'

Timer 4 Binary Counter

8-bit access register (16-bit access is possible from even address.)

TM4BC is a read-only register.

7	6	5	4	3	2	1	0
TM4 BC7	TM4 BC6	TM4 BC5	TM4 BC4	TM4 BC3	TM4 BC2	TM4 BC1	TM4 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Counter Value of Timer 4

TM5BC : x'00FE05'

Timer 5 Binary Counter

8-bit access register (16-bit access is possible from even address.)

TM5BC is a read-only register.

7	6	5	4	3	2	1	0
TM5 BC7	TM5 BC6	TM5 BC5	TM5 BC4	TM5 BC3	TM5 BC2	TM5 BC1	TM5 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Counter Value of Timer 5

7	6	5	4	3	2	1	0
TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM0BR : x'00FE10'

Timer 0 Base Register

8/16-bit access register

7:0 Timer 0 Count Cycle Count cycle (2 to 256) is set. Setting value +1 is counted. Set between 1 to 255.

It is possible to set 0 after activation. For detail, refer to "4-2 8-bit Timer Setup Examples"

7	6	5	4	3	2	1	0
TM1 BR7	TM1 BR6	TM1 BR5	TM1 BR4	TM1 BR3	TM1 BR2	TM1 BR1	TM1 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM1BR : x'00FE11'

Timer 1 Base Register

8-bit access register (16-bit access is possible from even address.)

7:0 Timer 1 Count Cycle Count cycle (2 to 256) is set. Setting value +1 is counted. Set between 1 to 255.

It is possible to set 0 after activation. For detail, refer to "4-2 8-bit Timer Setup Examples"

7	6	5	4	3	2	1	0
TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM2BR : x'00FE12'

Timer 2 Base Register

8/16-bit access register

7:0 Timer 2 Count Cycle Count cycle (2 to 256) is set. Setting value +1 is counted. Set between 1 to 255.

It is possible to set 0 after activation. For detail, refer to "4-2 8-bit Timer Setup Examples"

TM3BR : x'00FE13'

Timer 3 Base Register

8-bit access register
(16-bit access is possible from even address.)

It is possible to set 0 after activation. For detail, refer to "4-2 8-bit Timer Setup Examples"

7	6	5	4	3	2	1	0
TM3 BR7	TM3 BR6	TM3 BR5	TM3 BR4	TM3 BR3	TM3 BR2	TM3 BR1	TM3 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 3 Count Cycle Count cycle (2 to 256) is set. Setting value +1 is counted. Set between 1 to 255.

TM4BR : x'00FE14'

Timer 4 Base Register

8/16-bit access register

It is possible to set 0 after activation. For detail, refer to "4-2 8-bit Timer Setup Examples"

7	6	5	4	3	2	1	0
TM4 BR7	TM4 BR6	TM4 BR5	TM4 BR4	TM4 BR3	TM4 BR2	TM4 BR1	TM4 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 4 Count Cycle Count cycle (2 to 256) is set. Setting value +1 is counted. Set between 1 to 255.

T

TM5BR : x'00FE15'

Timer 5 Base Register

8-bit access register
(16-bit access is possible from even address.)

It is possible to set 0 after activation. For detail, refer to "4-2 8-bit Timer Setup Examples"

7	6	5	4	3	2	1	0
TM5 BR7	TM5 BR6	TM5 BR5	TM5 BR4	TM5 BR3	TM5 BR2	TM5 BR1	TM5 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 5 Count Cycle Count cycle (2 to 256) is set. Setting value +1 is counted. Set between 1 to 255.

TM0MD : x'00FE20'

Timer 0 Mode Register

8/16-bit access register

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	-	-	-	-	TM0 S1	TM0 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

Bit	Name	Description
7	**Timer 0 Count Operation Control**	0: Count stops 1: Operation
6	**Timer 0 Base Register Setup**	0: Do nothing 1: Set TM0BR to TM0BC 2 dividing circuit reset Fix TMIO output to 0
1:0	**Clock Source**	00: TM0IO pin clock (event timer) 01: 128 dividing clock of system clock 10: System clock 11: 64 dividing clock of system clock

TM1MD : x'00FE21'

Timer 1 Mode Register

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
TM1 EN	TM1 LD	-	-	-	-	TM1 S1	TM1 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

Bit	Name	Description
7	**Timer 1 Count Operation Control**	0: Count stops 1: Operation
6	**Timer 1 Base Register Setup**	0: Do nothing 1: Set TM1BR to TM1BC 2 dividing circuit reset Fix TMIO output to 0
1:0	**Clock Source**	00: TM1IO pin clock (event timer) 01: 64 dividing clock of system clock 10: Timer 0 output clock 11: System clock

TM2MD : x'00FE22'

Timer 2 Mode Register

8/16-bit access register

7	6	5	4	3	2	1	0
TM2 EN	TM2 LD	-	-	-	-	TM2 S1	TM2 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

7 Timer 2 Count Operation Control

0: Count stops 1: Operation

6 Timer 2 Base Register Setup

0: Do nothing
1: Set TM2BR to TM2BC
2 dividing circuit reset
Fix TMIO output to 0

1:0 Clock Source

00: TM2IO pin clock (event timer)
01: Timer 1 cascade connection
10: Timer 0 output clock
11: System clock

TM3MD : x'00FE23'

Timer 3 Mode Register

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
TM3 EN	TM3 LD	-	-	-	-	TM3 S1	TM3 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

7 Timer 3 Count Operation Control

0: Count stops 1: Operation

6 Timer 3 Base Register Setup

0: Do nothing
1: Set TM3BR to TM3BC
2 dividing circuit reset

1:0 Clock Source

00: 64 dividing clock of system clock
01: 2 dividing clock of system clock
10: Timer 0 output clock
11: System clock

TM4MD : x'00FE24'

Timer 4 Mode Register

8/16-bit access register

7	6	5	4	3	2	1	0
TM4 EN	TM4 LD	-	-	-	-	TM4 S1	TM4 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

7 Timer 4 Count Operation Control
0: Count stops 1: Operation

6 Timer 4 Base Register Setup
0: Do nothing
1: Set TM4BR to TM4BC
2 dividing circuit reset

1:0 Clock Source
00: 128 dividing clock of system clock
01: 64 dividing clock of system clock
10: Timer 0 output clock
11: System clock

TM5MD : x'00FE25'

Timer 5 Mode Register

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
TM5 EN	TM5 LD	-	-	-	-	TM5 S1	TM5 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

7 Timer 5 Count Operation Control
0: Count stops 1: Operation

6 Timer 5 Base Register Setup
0: Do nothing
1: Set TM5BR to TM5BC
2 dividing circuit reset

1:0 Clock Source
00: 64 dividing clock of system clock
01: Timer 4 cascade connection
10: Timer 0 output clock
11: System clock

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	-	-	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	-	TM6 LP	TM6 ASEL	-	TM6 S1	TM6 S0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0	0/1	0/1

TM6MD : x'00FE30'

Timer 6 Mode Register

16-bit access register

15 Timer 6BC Count Operation Control
0: Disable 1: Enable

14 Operation Selection of TM6BC, T.F.F, RS.F.F
0: Clear 1: Operation

11:10 Up/down Operation
00: Up counter
01: Down counter
10: Up at TM6IO=1, down at TM6IO=0
11: Setup is inhibited.

9 Count Start External Enable
0: Inhibited 1:External trigger *

** Set TM6EN at TM6IO (↓) (Set to '1' only at interval timer). Clear TM6EN at TM6BC=TM6CA.*

8 Iteration/ One Shot Operation
0: Iteration 1: One shot operation

7:6 TM6CA, B Operation Mode
00: Use compare register (single buffer)
01: Use compare register (double buffer)
10: Use capture register
TM6IO (↑): capture A
TM6IO (↓): capture B
11: Setup is inhibited.

4 Clear TM6BC or Reload TM6CA Value
On up-counter setup at TM6BC=TM6CA
0: Not clear TM6BC value
1: Clear TM6BC value *
On down-counter setup at TM6BC=0
0: Not reload TM6CA
1: Reload TM6CA *

** Used for PWM output*

** Used for 16-bit reload timer. At TM6LP=1 on up-counter, if TM6BC matches TM6CA, or count to x'FFFF', TM6BC is cleared to '0' at the next cycle. At down-counter, if TM6BC gets to '0', TM6BC is set to the value of TM6CA at the next cycle regardless of operation setup.*

3 Output to TM6IO
0: RS.F.F 1: T.F.F

1:0 Clock Source
00: Timer 0 output clock
01: 128 dividing clock of system clock
10: TM6IO pin clock
11: System clock

T

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 BC15	TM6 BC14	TM6 BC13	TM6 BC12	TM6 BC11	TM6 BC10	TM6 BC9	TM6 BC8	TM6 BC7	TM6 BC6	TM6 BC5	TM6 BC4	TM6 BC3	TM6 BC2	TM6 BC1	TM6 BC0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/10	0/1	0/1

TM6BC : x'00FE32'

Timer 6 Binary Counter

16-bit access register

15:0 Timer 6 Count Value

TM6BC is a read-only register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CA15	TM6 CA14	TM6 CA13	TM6 CA12	TM6 CA11	TM6 CA10	TM6 CA9	TM6 CA8	TM6 CA7	TM6 CA6	TM6 CA5	TM6 CA4	TM6 CA3	TM6 CA2	TM6 CA1	TM6 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM6CA : x'00FE34'

Timer 6 Compare Capture Register A

16-bit access register

15:0 Timer 6 Count Cycle Set count cycle -1

The value that was captured can be read at capture setup. Set PWM cycle at compare setup.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CAX15	TM6 CAX14	TM6 CAX13	TM6 CAX12	TM6 CAX11	TM6 CAX10	TM6 CAX9	TM6 CAX8	TM6 CAX7	TM6 CAX6	TM6 CAX5	TM6 CAX4	TM6 CAX3	TM6 CAX2	TM6 CAX1	TM6 CAX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

TM6CAX : x'00FE36'

Timer 6 Compare Capture Register Set A

16-bit access register

15:0 This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM6CA is read by write-signal of this register, and PWM cycle is determined by TM6CAX. When TM6BC matches the value of TM6CAX, the value of TM6CA is read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CB15	TM6 CB14	TM6 CB13	TM6 CB12	TM6 CB11	TM6 CB10	TM6 CB9	TM6 CB8	TM6 CB7	TM6 CB6	TM6 CB5	TM6 CB4	TM6 CB3	TM6 CB2	TM6 CB1	TM6 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM6CB : x'00FE38'

Timer 6 Compare Capture Register B

16-bit access register

15:0 Change of PWM

The value that was captured can be read at capture setup. Set PWM duty at compare setup.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CBX15	TM6 CBX14	TM6 CBX13	TM6 CBX12	TM6 CBX11	TM6 CBX10	TM6 CBX9	TM6 CBX8	TM6 CBX7	TM6 CBX6	TM6 CBX5	TM6 CBX4	TM6 CBX3	TM6 CBX2	TM6 CBX1	TM6 CBX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

TM6CBX : x'00FE3A'

Timer 6 Compare Capture Register Set B

16-bit access register

15:0

This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM6CB is read by write-signal of this register, and PWM duty is determined by TM6CBX. When TM6BC matches the value of TM6CAX, the value of TM6CB is read.

T

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7 NLD	-	-	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	-	TM7 LP	TM7 ASEL	-	TM7 S1	TM7 S0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0	0/1	0/1

TM7MD : x'00FE40'

Timer 7 Mode Register

16-bit access register

15 Count Operation Control of TM7BC
0: Disable 1: Enable

14 Operation Selection of TM7BC, T.F.F, RS.F.F
0: Clear 1: Operation

11:10 Up/Down Operation
00: Up counter
01: Down counter
10: Up at TM7IO=1, down at TM7IO=0
11: Setup is inhibited.

9 Count Start External Enable
0: Inhibited 1: External trigger *

** Set TM7EN at TM7IO (↓) (Set to '1' only at interval timer). Clear TM7EN at TM7BC=TM7CA.*

8 Iteration/One shot Operation
0: Iteration 1: One shot operation

7:6 TM7CA, B Operation Mode
00: Use compare register (single buffer)
01: Use compare register (double buffer)
10: Use capture register
TM7IO (↑): capture A
TM7IO (↓): capture B
11: Setup is inhibited.

4 Clear TM7BC or Reload the Value of TM7CA
On up-counter setup at TM7BC=TM7CA
0: Not clear TM7BC
1: Clear TM7BC *
On down-counter setup at TM7BC=0
0: Not reload TM7CA value
1: Reload TM7CA value *

** Used for PWM output*

** Used for 16-bit reload timer. At TM7LP=1 on up-counter, if TM7BC matches TM7CA, or count to x'FFFF', TM7BC is cleared to '0' at the next cycle. At down-counter, if TM7BC gets to '0', TM7BC is set to the value of TM7CA at the next cycle regardless of operation setup.*

3 Output to TM7IO
0: RS.F.F 1: T.F.F

1:0 Clock Source
00: Timer 0 output clock
01: 128 dividing clock of system clock
10: TM7IO pin clock
11: System clock

TM7BC : x'00FE42'

Timer 7 Binary Counter

16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 BC15	TM7 BC14	TM7 BC13	TM7 BC12	TM7 BC11	TM7 BC10	TM7 BC9	TM7 BC8	TM7 BC7	TM7 BC6	TM7 BC5	TM7 BC4	TM7 BC3	TM7 BC2	TM7 BC1	TM7 BC0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15:0 Timer 7 Count Value

TM7BC is a read-only register.

TM7CA : x'00FE44'

Timer 7 Compare Capture Register A

16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CA15	TM7 CA14	TM7 CA13	TM7 CA12	TM7 CA11	TM7 CA10	TM7 CA9	TM7 CA8	TM7 CA7	TM7 CA6	TM7 CA5	TM7 CA4	TM7 CA3	TM7 CA2	TM7 CA1	TM7 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

15:0 Timer 7 Count Cycle Set count cycle -1

The value that was captured can be read at capture setup. Set PWM cycle at compare setup.

TM7CAX : x'00FE46'

Timer 7 Compare Capture Register Set A

16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CAX15	TM7 CAX14	TM7 CAX13	TM7 CAX12	TM7 CAX11	TM7 CAX10	TM7 CAX9	TM7 CAX8	TM7 CAX7	TM7 CAX6	TM7 CAX5	TM7 CAX4	TM7 CAX3	TM7 CAX2	TM7 CAX1	TM7 CAX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15:0 This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM7CA is read by write-signal of this register, and PWM cycle is determined by TM7CAX. When TM7BC matches the value of TM7CAX, the value of TM7CA is read.

T

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CB15	TM7 CB14	TM7 CB13	TM7 CB12	TM7 CB11	TM7 CB10	TM7 CB9	TM7 CB8	TM7 CB7	TM7 CB6	TM7 CB5	TM7 CB4	TM7 CB3	TM7 CB2	TM7 CB1	TM7 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM7CB : x'00FE48'

Timer 7 Compare Capture Register B

16-bit access register

15:0 Change of PWM

The value that was captured can be read at capture setup. Set PWM duty at compare setup.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CBX15	TM7 CBX14	TM7 CBX13	TM7 CBX12	TM7 CBX11	TM7 CBX10	TM7 CBX9	TM7 CBX8	TM7 CBX7	TM7 CBX6	TM7 CBX5	TM7 CBX4	TM7 CBX3	TM7 CBX2	TM7 CBX1	TM7 CBX0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

TM7CBX : x'00FE4A'

Timer 7 Compare Capture Register Set B

16-bit access register

15:0 This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM7CB is read by write-signal of this register, and PWM duty is determined by TM7CBX. When TM7BC matches the value of TM7CAX, the value of TM7CB is read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM8 EN	TM8 NLD	-	-	TM8 UD1	TM8 UD0	TM8 TGE	TM8 ONE	TM8 MD1	TM8 MD0	-	TM8 LP	TM8 ASEL	-	TM8 S1	TM8 S0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0	0/1	0/1

TM8MD : x'00FE50'

Timer 8 Mode Register

16-bit access register

15 Count Operation Control of TM8BC 0: Disable 1: Enable

14 Operation Selection of TM8BC, T.F.F, RS.F.F 0: Clear 1: Operation

11:10 Up/Down Operation
00: Up counter
01: Down counter
10: Up at TM8IO=1, down at TM8IO=0
11: Setup is inhibited.

9 Count Start External Enable 0: Inhibited 1: External trigger *

** Set TM8EN at TM8IO (↓) (Set to '1' only at interval timer). Clear TM8EN at TM8BC=TM8CA.*

8 Iteration/One shot Operation 0: Iteration 1: One shot operation

7:6 TM8CA, B Operation Mode
00: Use compare register (single buffer)
01: Use compare register (double buffer)
10: Use capture register
TM8IO (↑): capture A
TM8IO (↓): capture B
11: Setup is inhibited.

4 Clear TM8BC or Reload the Value of TM8CA
On up-counter setup at TM8BC=TM8CA
0: Not clear TM8BC
1: Clear TM8BC *
On down-counter setup at TM8BC=0
0: Not reload TM8CA value
1: Reload TM8CA value *

** Used for PWM output*

** Used for 8 bit reload timer.*

At TM8LP=1 on up-counter, if TM8BC matches TM8CA, or count to x'FFFF', TM8BC is cleared to '0' at the next cycle. At down-counter, if TM8BC gets to '0', TM8BC is set to the value of TM8CA at the next cycle regardless of operation setup.

3 Output to TM8IO 0: RS.F.F 1: T.F.F

1:0 Clock Source
00: Timer 0 output clock
01: 8 dividing clock of system clock
10: TM8IO pin clock
11: System clock 2 dividing

T

TM8BC : x'00FE52'

Timer 8 Binary Counter

8-bit access register

7	6	5	4	3	2	1	0
TM8 BC7	TM8 BC6	TM8 BC5	TM8 BC4	TM8 BC3	TM8 BC2	TM8 BC1	TM8 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 8 Count Value

TM8BC is a read-only register.

TM8CA : x'00FE54'

Timer 8 Compare Capture Register A

8-bit access register

7	6	5	4	3	2	1	0
TM8 CA7	TM8 CA6	TM8 CA5	TM8 CA4	TM8 CA3	TM8 CA2	TM8 CA1	TM8 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 8 Count Cycle Set count cycle -1

The value that was captured can be read at capture setup. Set PWM cycle at compare setup.

TM8CAX : x'00FE56'

Timer 8 Compare Capture Register Set A

8-bit access register

7	6	5	4	3	2	1	0
TM8 CAX7	TM8 CAX6	TM8 CAX5	TM8 CAX4	TM8 CAX3	TM8 CAX2	TM8 CAX1	TM8 CAX0
-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-

7:0 This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM8CA is read by write-signal of this register, and PWM cycle is determined by TM8CAX. When TM8BC matches the value of TM8CAX, the value of TM8CA is read.

TM8CB : x'00FE58'

Timer 8 Compare Capture Register B

8-bit access register

7	6	5	4	3	2	1	0
TM8 CB7	TM8 CB6	TM8 CB5	TM8 CB4	TM8 CB3	TM8 CB2	TM8 CB1	TM8 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The value that was captured can be read at capture setup. Set PWM duty at compare setup.

7:0 Change of PWM

TM8CBX : x'00FE5A'

Timer 8 Compare Capture Register Set B

8-bit access register

7	6	5	4	3	2	1	0
TM8 CBX7	TM8 CBX6	TM8 CBX5	TM8 CBX4	TM8 CBX3	TM8 CBX2	TM8 CBX1	TM8 CBX0
-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-

When compare register is set to double buffer, the value of TM8CB is read by write-signal of this register, and PWM duty is determined by TM8CBX. When TM8BC matches the value of TM8CAX, the value of TM8CB is read.

7:0 This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

T

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM9 EN	TM9 NLD	-	-	TM9 UD1	TM9 UD0	TM9 TGE	TM9 ONE	TM9 MD1	TM9 MD0	-	TM9 LP	TM9 ASEL	-	TM9 S1	TM9 S0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0	0/1	0/1

TM9MD : x'00FE60'

Timer 9 Mode Register

16-bit access register

15 Count Operation Control of TM9BC
0: Disable 1: Enable

14 Operation Selection of TM9BC, T.F.F, RS.F.F
0: Clear 1: Operation

11:10 Up/Down Operation
00: Up counter
01: Down counter
10: Up at TM9IO=1, down at TM9IO=0
11: Setup is inhibited.

9 Count Start External Enable
0: Inhibited 1: External trigger *

** Set TM9EN at TM9IO (↓) (Set to '1' only at interval timer). Clear TM9EN at TM9BC=TM9CA.*

8 Iteration/One shot Operation
0: Iteration 1: One shot operation

7:6 TM9CA, B Operation Mode
00: Use compare register (single buffer)
01: Use compare register (double buffer)
10: Use capture register
TM9IO (↑): capture A
TM9IO (↓): capture B
11: Setup is inhibited.

4 Clear TM9BC or Reload the Value of TM9CA
On up-counter setup at TM9BC=TM9CA
0: Not clear TM9BC
1: Clear TM9BC *
On down-counter setup at TM9BC=0
0: Not reload TM9CA value
1: Reload TM9CA value*

** Used for PWM output*

** Used for 8 bit reload timer. At TM9LP=1 on up-counter, if TM9BC matches TM9CA, or count to x'FFFF', TM9BC is cleared to '0' at the next cycle. At down-counter, if TM9BC gets to '0', TM9BC is set to the value of TM9CA at the next cycle regardless of operation setup.*

3 Output to TM9IO
0: RS.F.F 1: T.F.F

1:0 Clock Source
00: Timer 0 output clock
01: 8 dividing clock of system clock
10: TM9IO pin clock
11: System clock 2 dividing

7	6	5	4	3	2	1	0
TM9 BC7	TM9 BC6	TM9 BC5	TM9 BC4	TM9 BC3	TM9 BC2	TM9 BC1	TM9 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM9BC : x'00FE62'

Timer 9 Binary Counter

8-bit access register

7:0 Timer 9 Count Value

TM9BC is a read-only register.

7	6	5	4	3	2	1	0
TM9 CA7	TM9 CA6	TM9 CA5	TM9 CA4	TM9 CA3	TM9 CA2	TM9 CA1	TM9 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM9CA : x'00FE64'

Timer 9 Compare Capture Register A

8-bit access register

7:0 Timer 9 Count Cycle Set count cycle -1

The value that was captured can be read at capture setup. Set PWM cycle at compare setup.

7	6	5	4	3	2	1	0
TM9 CAX7	TM9 CAX6	TM9 CAX5	TM9 CAX4	TM9 CAX3	TM9 CAX2	TM9 CAX1	TM9 CAX0
-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-

TM9CAX : x'00FE66'

Timer 9 Compare Capture Register Set A

8-bit access register

7:0 This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM9CA is read by write-signal of this register, and PWM cycle is determined by TM9CAX. When TM9BC matches the value of TM9CAX, the value of TM9CA is read.

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TM9CB : x'00FE68'

Timer 9 Compare Capture Register B

8-bit access register

7	6	5	4	3	2	1	0
TM9 CB7	TM9 CB6	TM9 CB5	TM9 CB4	TM9 CB3	TM9 CB2	TM9 CB1	TM9 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Change of PWM

The value that was captured can be read at capture setup. Set PWM duty at compare setup.

TM9CBX : x'00FE6A'

Timer 9 Compare Capture Register Set B

8-bit access register

7	6	5	4	3	2	1	0
TM9 CBX7	TM9 CBX6	TM9 CBX5	TM9 CBX4	TM9 CBX3	TM9 CBX2	TM9 CBX1	TM9 CBX0
-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-

7:0

This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM9CB is read by write-signal of this register, and PWM duty is determined by TM9CBX. When TM9BC matches the value of TM9CAX, the value of TM9CB is read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM10 EN	TM10 NLD	-	TM10 SEL	-	TM10 UD0	-	TM10 ONE	-	TM10 MD0	-	TM10 LP	-	-	TM10 S1	TM10 S0
R/W	R/W	R	R/W	R	R/W	R	R/W	R	R/W	R	R/W	R	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0/1	0	0/1	0	0/1	0	0/1	0	0/1	0	0	0/1	0/1

TM10MD : x'00FE70'

Timer 10 Mode Register

16-bit access register

15 Count Operation Control of TM10BC
0: Disable 1: Enable

14 Operation Selection of TM10BC, T.F.F, RS.F.F
0: Clear 1: Operation

12 PWM Cycle, Interrupt Selection
0: Compare register A match
1: TM10BC overflow

10 Up/Down Operation
0: Up counter 1: Down counter

8 Iteration/One shot Operation
0: Iteration 1: One shot operation

6 TM10CA, B Operation Mode
0: Use compare register (single buffer)
1: Use compare register (double buffer)

4 Clear TM10BC or Reload the Value of TM10CA
On up-counter setup at TM10BC=TM10CA
0: Not clear TM10BC
1: Clrea TM10BC *
On down-counter setup at TM10BC=0
0: Not reload TM10CA value
1: Reload TM10CA value *

** Used for PWM output*

** Used for 8 bit reload timer.*
At TM10LP=1 on up-counter, if TM10BC matches TM10CA, or count to x'FFFF', TM10BC is cleared to '0' at the next cycle. At down-counter, if TM10BC gets to '0', TM10BC is set to the value of TM10CA at the next cycle regardless of operation setup.

1:0 Clock Source
00: Internal OSC clock
01: 8 dividing clock of system clock
10: System clock
11: 2 dividing clock of system clock

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TM10BC : x'00FE72'

Timer 10 Binary Counter

8-bit access register

7	6	5	4	3	2	1	0
TM10 BC7	TM10 BC6	TM10 BC5	TM10 BC4	TM10 BC3	TM10 BC2	TM10 BC1	TM10 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 10 Count Value

TM10BC is a read-only register.

TM10CA : x'00FE74'

Timer 10 Compare Capture Register A

8-bit access register

7	6	5	4	3	2	1	0
TM10 CA7	TM10 CA6	TM10 CA5	TM10 CA4	TM10 CA3	TM10 CA2	TM10 CA1	TM10 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 10 Count Cycle Set count cycle -1

Set PWM cycle at compare setup.

TM10CAX : x'00FE76'

Timer 10 Compare Capture Register Set A

8-bit access register

7	6	5	4	3	2	1	0
TM10 CAX7	TM10 CAX6	TM10 CAX5	TM10 CAX4	TM10 CAX3	TM10 CAX2	TM10 CAX1	TM10 CAX0
-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-

7:0 This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM10CA is read by write-signal of this register, and PWM cycle is determined by TM10CAX. When TM10BC matches the value of TM10CAX, the value of TM10CA is read.

TM10CB : x'00FE78'

Timer 10 Compare Capture Register B

8-bit access register

7	6	5	4	3	2	1	0
TM10 CB7	TM10 CB6	TM10 CB5	TM10 CB4	TM10 CB3	TM10 CB2	TM10 CB1	TM10 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Change of PWM

Set PWM duty at compare setup.

TM10CBX : x'00FE7A'

Timer 10 Compare Capture Register Set B

8-bit access register

7	6	5	4	3	2	1	0
TM10 CBX7	TM10 CBX6	TM10 CBX5	TM10 CBX4	TM10 CBX3	TM10 CBX2	TM10 CBX1	TM10 CBX0
-	-	-	-	-	-	-	-
0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-

7:0

This can not be read or written as a register, but gets to be available only when compare register is set to double buffer.

When compare register is set to double buffer, the value of TM10CB is read by write-signal of this register, and PWM duty is determined by TM10CBX. When TM10BC matches the value of TM10CAX, the value of TM10CB is read.

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	TM11 ADS	TM11 SDSA	TM11 SDSB	TM11 PCRA	TM11 PCRB	TM11 INTA	TM11 INTB	TM11 DTEN	TM11 ORMD	TM11 CEN	TM11 WVM
R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM11MD : x'00FE80'

Timer 11 Mode Control Register

16-bit access register

Mode setup of 6-phase inverter motor control block

10 **Selection of A/D Signal Start-up Factor**
0: 16-bit counter value = cycle setup register value
1: Underflow of 16-bit counter

9 **Buffer Mode Selection of TM11EX (Output Polarity Control Register)**
0: Single buffer
1: Double buffer

8 **Buffer Mode Selection of TM11SL (Output Control Setup Register)**
0: Single buffer
1: Double buffer

7 **Load Timing Permission of Double Buffer (at Underflow of 16-bit Counter)**
0: Disable 1: Enable

6 **Load Timing Permission of Double Buffer (at 16-bit Counter Value = Cycle Setup Register Value)**
0: Disable 1: Enable

5 **Underflow Interrupt Permission of 16-bit Counter**
0: Disable 1: Enable

4 **Unison Interrupt Permission of 16-bit Counter and Cycle Setup Register**
0: Disable 1: Enable

3 **Permission of Dead Time Insert**
0: Disable 1: Enable

2 **Switch of Output Logic (At Dead Time Insert)**
0: Positive logic 1: Negative logic

1 **16-bit Counter Operation Control**
0: Disable 1: Enable

0 **Selection of Waveform**
0: Triangular waveform
1: Sawtooth waveform

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	TM11 WS	TM11 VS	TM11 US
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

TM11EX : x'00FE82'

Timer 11 Output Polarity Control Register

16-bit access register

TM11MD register can select the switch of double buffer or single buffer.
When double buffer is selected, the register value is loaded at the timing set at TM11MD.
When counter is stopped, the value of double buffer is equal to the register value regardless of setup of load timing.

2	**W-phase Output Polarity Selection (PWM2)**	0: Positive phase	1: Negative phase
1	**V-phase Output Polarity Selection (PWM1)**	0: Positive phase	1: Negative phase
0	**U-phase Output Polarity Selection (PWM0)**	0: Positive phase	1: Negative phase

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	TM11 PSNW	TM11 PSW	TM11 PSNV	TM11 PSV	TM11 PSNU	TM11 PSU	TM11 LVNW	TM11 LVW	TM11 LVNV	TM11 LVV	TM11 LVNU	TM11 LVU
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM11SL : x'00FE84'

Timer 11 Output Control Register

16-bit access register

11 **Output Source Selection of NW ($\overline{\text{PWM2}}$)** 0: PWM output 1: Fixed output

Select output mode from PWM output or fixed output. When fixed output is selected, 'H' or 'L' can be selected to be fixed.

10 **Output Source Selection of W (PWM2)** 0: PWM output 1: Fixed output

9 **Output Source Selection of NV ($\overline{\text{PWM1}}$)** 0: PWM output 1: Fixed output

8 **Output Source Selection of V (PWM1)** 0: PWM output 1: Fixed output

7 **Output Source Selection of NU ($\overline{\text{PWM0}}$)** 0: PWM output 1: Fixed output

6 **Output Source Selection of U (PWM0)** 0: PWM output 1: Fixed output

5 **Level Selection of NW ($\overline{\text{PWM2}}$) fixed Output** 0: Fixed to 'L' 1: Fixed to 'H'

4 **Level Selection of W (PWM2) fixed Output** 0: Fixed to 'L' 1: Fixed to 'H'

3 **Level Selection of NV ($\overline{\text{PWM1}}$) fixed Output** 0: Fixed to 'L' 1: Fixed to 'H'

2 **Level Selection of V (PWM1) fixed Output** 0: Fixed to 'L' 1: Fixed to 'H'

1 **Level Selection of NU ($\overline{\text{PWM0}}$) fixed Output** 0: Fixed to 'L' 1: Fixed to 'H'

0 **Level Selection of U (PWM0) fixed Output** 0: Fixed to 'L' 1: Fixed to 'H'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 BR15	TM11 BR14	TM11 BR13	TM11 BR12	TM11 BR11	TM11 BR10	TM11 BR09	TM11 BR08	TM11 BR07	TM11 BR06	TM11 BR05	TM11 BR04	TM11 BR03	TM11 BR02	TM11 BR01	TM11 BR00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM11BR : x'00FE86'

Timer 11 Cycle Setup Register

16-bit access register

15:0 Set the cycle of PWM 16-bit counter

Set the cycles of PWM0 (U-phase), PWM1 (V-phase) and PWM2 (W-phase).
This register is double buffer setup only. The register value is loaded to PWM at the timing set at TM11MD.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CA15	TM11 CA14	TM11 CA13	TM11 CA12	TM11 CA11	TM11 CA10	TM11 CA09	TM11 CA08	TM11 CA07	TM11 CA06	TM11 CA05	TM11 CA04	TM11 CA03	TM11 CA02	TM11 CA01	TM11 CA00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM11CA : x'00FE88'

Timer 11 U-phase Comparison Setup Register

16-bit access register

15:0 Set the Value Which is Compared to PWM 16-bit Counter (Duty Setup)

Determine the output duty of PWM 0 (U-phase).
This register is double buffer setup only. The register value is loaded to PWM at the timing set at TM11MD.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CB15	TM11 CB14	TM11 CB13	TM11 CB12	TM11 CB11	TM11 CB10	TM11 CB09	TM11 CB08	TM11 CB07	TM11 CB06	TM11 CB05	TM11 CB04	TM11 CB03	TM11 CB02	TM11 CB01	TM11 CB00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM11CB : x'00FE8A'

Timer 11 V-phase Comparison Setup Register

16-bit access register

15:0 Set the Value Which is Compared to PWM 16-bit Counter (Duty Setup)

Determine the output duty of PWM1 (V-phase).
This register is double buffer setup only. The register value is loaded to PWM at the timing set at TM11MD.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM11 CC15	TM11 CC14	TM11 CC13	TM11 CC12	TM11 CC11	TM11 CC10	TM11 CC09	TM11 CC08	TM11 CC07	TM11 CC06	TM11 CC05	TM11 CC04	TM11 CC03	TM11 CC02	TM11 CC01	TM11 CC00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM11CC : x'00FE8C'

Timer 11 W-phase Comparison Setup Register

16-bit access register

15:0 Set the Value Which is Compared to PWM 16-bit Counter (Duty Setup)

Determine the output duty of PWM 1 (W-phase).
This register is double buffer setup only. The register value is loaded to PWM at the timing set at TM11MD.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	TM11 DT07	TM11 DT06	TM11 DT05	TM11 DT04	TM11 DT03	TM11 DT02	TM11 DT01	TM11 DT00
R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM11DT : x'00FE8E'

Timer 11 Dead Time Setup Register

16-bit access register

7:0 Set the Value of 8-bit Counter for Dead Time Generation

Set the dead time of PWM0 (U-phase), PWM1 (V-phase) and PWM2 (W-phase).
This register is double buffer setup only. The register value is loaded to PWM at the timing set at TM11MD.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TM11 CK0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1

TM11CK : x'00FE90'

Timer 11 Clock Source Selection Register

16-bit access register

0

0: Internal clock
1: System clock

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	PM SEL11	PM SEL10	PM SEL9	PM SEL8	PM SEL7	PM SEL6	PM SEL5	PM SEL4	PM SEL3	PM SEL2	PM SEL1	PM SEL0
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

PMSEL: x'00FFA0'

Multi-port Selection Register

8/16-bit access register

Use always this register when the registers following are used. They are SBT0, SBI0, SBO0, TM0IO, TM1IO, TM2IO, TM6IO, TM7IO, AN4, AN5, AN6, AN7, AN8, AN9, AN10 and AN11.

11 Analog Input Multiple Selection 0: Select AN7 1: Select AN11

10 Analog Input Multiple Selection 0: Select AN6 1: Select AN10

9 Analog Input Multiple Selection 0: Select AN5 1: Select AN9

8 Analog Input Multiple Selection 0: Select AN4 1: Select AN8

7 Timer Pin Multiple Selection
0: Use P14 as TM7IO
1: Use P44 as TM7IO

When each 7 to 0 bits of PMSEL register are '0', it is inhibited to set TM0IO, TM1IO, TM2IO, TM6IO by P4MDA.
It is also inhibited to set TM7IO by P4MDB, and SBT0 and SBO0 by P6MDA.

6 Timer Pin Multiple Selection
0: Use P13 as TM6IO
1: Use P43 as TM6IO

5 Timer Pin Multiple Selection
0: Use P12 as TM2IO
1: Use P42 as TM2IO

4 Timer Pin Multiple Selection
0: Use P11 as TM1IO
1: Use P41 as TM1IO

3 Timer Pin Multiple Selection
0: Use P10 as TM0IO
1: Use P40 as TM0IO

2 Serial Pin Multiple Selection
0: Use P02 as SBO0
1: Use P62 as SBO0

When each 7 to 0 bits of PMSEL are '1', it is inhibited to set SBT0 and SBO0 by P0MD.
It is also inhibited to set TM0IO, TM1IO, TM2IO and TM6IO by P1MDA, and TM7IO by P1MDB.

1 Serial Pin Multiple Selection
0: Use P01 as SBI0
1: Use P61 as SBI0

0 Serial Pin Multiple Selection
0: Use P00 as SBT0
1: Use P60 as SBT0

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	AN SEL11	AN SEL10	AN SEL9	AN SEL8	AN SEL7	AN SEL6	AN SEL5	AN SEL4	AN SEL3	AN SEL2	AN SEL1	AN SEL0
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

ANSEL: x'00FFA2'

Analog Port Selection Register

8/16-bit access register

Set always ANSEL register to '1' when AN0 to AN11 are used.

11 **Selection of AN8 (P57)** 0: Used as a port
1: Used as AN8

10 **Selection of AN9 (P56)** 0: Used as a port
1: Used as AN9

9 **Selection of AN10 (P55)** 0: Used as a port
1: Used as AN10

8 **Selection of AN11 (P54)** 0: Used as a port
1: Used as AN11

7 **Selection of AN0 (P37)** 0: Used as a port
1: Used as AN0

6 **Selection of AN1 (P36)** 0: Used as a port
1: Used as AN1

5 **Selection of AN2 (P35)** 0: Used as a port
1: Used as AN2

4 **Selection of AN3 (P34)** 0: Used as a port
1: Used as AN3

3 **Selection of AN4 (P33)** 0: Used as a port
1: Used as AN4

2 **Selection of AN5 (P32)** 0: Used as a port
1: Used as AN5

1 **Selection of AN6 (P31)** 0: Used as a port
1: Used as AN6

0 **Selection of AN7 (P30)** 0: Used as a port
1: Used as AN7

7	6	5	4	3	2	1	0
PPUP A7	*Note	PPUP A5	PPUP A4	PPUP A3	PPUP A2	PPUP A1	PPUP A0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0	0/1	0/1	0/1	0/1	0/1	0/1

* Note) Set always '0'.

PPUPA: x'00FFB0'

Port Pull-up Control A Register

8/16-bit access register

Set bit 6 always to '0'.

7	**Pull-up of P02 to P00 Pins**	0: None	1: Pull-up
5	**Pull-up of P53 to P50 Pins**	0: None	1: Pull-up
4	**Pull-up of P76 Pin**	0: None	1: Pull-up
3	**Pull-up of P75 Pin**	0: None	1: Pull-up
2	**Pull-up of P77, P74 to P72 Pins**	0: None	1: Pull-up
1	**Pull-up of P71 Pin**	0: None	1: Pull-up
0	**Pull-up of P70 (Buzz) Pin**	0: None	1: Pull-up

PPUPB: x'00FFB1'

Port Pull-up Control B Register

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
PPUP B7	PPUP B6	PPUP B5	PPUP B4	PPUP B3	PPUP B2	PPUP B1	PPUP B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7	**Pull-up of P25 ($\overline{IRQ5}$) Pin**	0: None	1: Pull-up
6	**Pull-up of P24 ($\overline{IRQ4}$) Pin**	0: None	1: Pull-up
5	**Pull-up of P23 ($\overline{IRQ3}$) Pin**	0: None	1: Pull-up
4	**Pull-up of P22 ($\overline{IRQ2}$) Pin**	0: None	1: Pull-up
3	**Pull-up of P21 ($\overline{IRQ1}$) Pin**	0: None	1: Pull-up
2	**Pull-up of P20 ($\overline{IRQ0}$) Pin**	0: None	1: Pull-up
1	**Pull-up of P16 and P16 Pins**	0: None	1: Pull-up
0	**Pull-up of P14 to P10 Pins**	0: None	1: Pull-up

7	6	5	4	3	2	1	0
-	-	-	-	*Note	PPUP C2	PPUP C1	PPUP C0
R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0	0/1	0/1	0/1

* Note) Set always '0'.

PPUPC: x'00FFB2'

Port Pull-up Control C Register

8/16-bit access register

Set bit 3 always to '0'.

2	**Pull-up of P65 to P63 (Serial) Pins**	0: None	1: Pull-up
1	**Pull-up of P62 to P60 (Serial) Pins**	0: None	1: Pull-up
0	**Pull-up of P45 to P40 Pins**	0: None	1: Pull-up

P

7	6	5	4	3	2	1	0
PPDW A7	PPDW A6	PPDW A5	PPDW A4	PPDW A3	PPDW A2	PPDW A1	PPDW A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

PPDWA: x'00FFB4'

Port Pull-down Control A Register

8/16-bit access register

7	**Pull-down of P37 (AN0) Pin**	0: None	1: Pull-down
6	**Pull-down of P36 (AN1) Pin**	0: None	1: Pull-down
5	**Pull-down of P35 (AN2) Pin**	0: None	1: Pull-down
4	**Pull-down of P34 (AN3) Pin**	0: None	1: Pull-down
3	**Pull-down of P33 (AN4) Pin**	0: None	1: Pull-down
2	**Pull-down of P32 (AN5) Pin**	0: None	1: Pull-down
1	**Pull-down of P31 (AN6) Pin**	0: None	1: Pull-down
0	**Pull-down of P30 (AN7) Pin**	0: None	1: Pull-down

7	6	5	4	3	2	1	0
-	-	-	-	PPDW B3	PPDW B2	PPDW B1	PPDW B0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1

PPDWB: x'00FFB5'

Port Pull-down Control B Register

8-bit access register (16-bit access is possible from even address.)

3	**Pull-down of P57 (AN8) Pin**	0: None	1: Pull-down
2	**Pull-down of P56 (AN9) Pin**	0: None	1: Pull-down
1	**Pull-down of P55 (AN10) Pin**	0: None	1: Pull-down
0	**Pull-down of P54 (AN11) Pin**	0: None	1: Pull-down

7	6	5	4	3	2	1	0
-	-	-	-	P0OUT3	P0OUT2	P0OUT1	P0OUT0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1

P0OUT : x'00FFC0'

Port 0 Output Register

8/16-bit access register

Software reset is possible at bit 3=0. After reset, the value is initialized.

3:0 Port 0 Output Data

7	6	5	4	3	2	1	0
-	P1OUT6	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P1OUT : x'00FFC1'

Port 1 Output Register

8-bit access register
(16-bit access is possible from even address.)

7:0 Port 1 Output Data

7	6	5	4	3	2	1	0
-	-	P2OUT5	P2OUT4	P2OUT3	P2OUT2	P2OUT1	P2OUT0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

P2OUT : x'00FFC2'

Port 2 Output Register

8/16-bit access register

5:0 Port 2 Output Data

7	6	5	4	3	2	1	0
P3OUT7	P3OUT6	P3OUT5	P3OUT4	P3OUT3	P3OUT2	P3OUT1	P3OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P3OUT : x'00FFC3'

Port 3 Output Register

8-bit access register
(16-bit access is possible from even address.)

7:0 Port 3 Output Data

P4OUT : x'00FFC4'

Port 4 Output Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P4OUT5	P4OUT4	P4OUT3	P4OUT2	P4OUT1	P4OUT0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 Port 4 Output Data

P5OUT : x'00FFC5'

Port 5 Output Register

8-bit access register
(16-bit access is possible
from even address.)

7	6	5	4	3	2	1	0
P5OUT7	P5OUT6	P5OUT5	P5OUT4	P5OUT3	P5OUT2	P5OUT1	P5OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 5 Output Data

P6OUT : x'00FFC6'

Port 6 Output Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 Port 6 Output Data

P

P7OUT : x'00FFC7'

Port 7 Output Register

8-bit access register
(16-bit access is possible

7	6	5	4	3	2	1	0
P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 7 Output Data

P0IN : x'00FFD0'

Port 0 Input Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	-	-	P0IN3	P0IN2	P0IN1	P0IN0
R	R	R	R	R	R	R	R
0	0	1	1	Port	Port	Port	Port
0	0	1	1	0/1	0/1	0/1	0/1

3:0 The value of Port 0 Pin

P1IN : x'00FFD1'

Port 1 Input Register

8-bit access register (16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
-	P1IN6	P1IN5	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0
R	R	R	R	R	R	R	R
0	Port	Port	Port	Port	Port	Port	Port
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

6:0 The value of Port 1 Pin

P2IN : x'00FFD2'

Port 2 Input Register

8/16-bit access register

The 6th bit is on the level of $\overline{NMI}$ pin.

7	6	5	4	3	2	1	0
-	NMI	P2IN5	P2IN4	P2IN3	P2IN2	P2IN1	P2IN0
R	R	R	R	R	R	R	R
0	NMI	Port	Port	Port	Port	Port	Port
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

5:0 The value of Port 2 Pin

P3IN : x'00FFD3'

Port 3 Input Register

8-bit access register (16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
P3IN7	P3IN6	P3IN5	P3IN4	P3IN3	P3IN2	P3IN1	P3IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 The value of Port 3 Pin

P4IN : x'00FFD4'

Port 4 Input Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P4IN5	P4IN4	P4IN3	P4IN2	P4IN1	P4IN0
R	R	R	R	R	R	R	R
0	0	Port	Port	Port	Port	Port	Port
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 The value of Port 4 Pin

P5IN : x'00FFD5'

Port 5 Input Register

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
P5IN7	P5IN6	P5IN5	P5IN4	P5IN3	P5IN2	P5IN1	P5IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 The value of Port 5 Pin

P6IN : x'00FFD6'

Port 6 Input Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0
R	R	R	R	R	R	R	R
0	0	Port	Port	Port	Port	Port	Port
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 The value of Port 6 Pin

P7IN : x'00FFD7'

Port 7 Input Register

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 The value of Port 7 Pin

P

P0DIR : x'00FFE0'

Port 0 I/O Control Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	*Note	*Note	-	P0DIR2	P0DIR1	P0DIR0
R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0	0/1	0/1	0/1

* Note) Set always '0'.

2:0 Each Bit I/O of Port 0 0: Input pin 1: Output pin

P1DIR : x'00FFE1'

Port 1 I/O Control Register

8-bit access register (16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
-	P1DIR6	P1DIR5	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

6:0 Each Bit I/O of Port 1 0: Input pin 1: Output pin

P2DIR : x'00FFE2'

Port 2 I/O Control Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P2DIR5	P2DIR4	P2DIR3	P2DIR2	P2DIR1	P2DIR0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 Each Bit I/O of Port 2 0: Input pin 1: Output pin

P3DIR : x'00FFE3'

Port 3 I/O Control Register

8-bit access register (16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
P3DIR7	P3DIR6	P3DIR5	P3DIR4	P3DIR3	P3DIR2	P3DIR1	P3DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Each Bit I/O of Port 3 0: Input pin 1: Output pin

P4DIR : x'00FFE4'

Port 4 I/O Control Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P4DIR5	P4DIR4	P4DIR3	P4DIR2	P4DIR1	P4DIR0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 **Each Bit I/O of Port 4** 0: Input pin 1: Output pin

P5DIR : x'00FFE5'

Port 5 I/O Control Register

8-bit access register (16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
P5DIR7	P5DIR6	P5DIR5	P5DIR4	P5DIR3	P5DIR2	P5DIR1	P5DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 **Each Bit I/O of Port 5** 0: Input pin 1: Output pin

P6DIR : x'00FFE6'

Port 6 I/O Control Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 **Each Bit I/O of Port 6** 0: Input pin 1: Output pin

P

P7DIR : x'00FFE7'

Port 7 I/O Control Register

8-bit access register (16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 **Each Bit I/O of Port 7** 0: Input pin 1: Output pin

P0MD : x'00FFF0'

Port 0 Output Mode Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	-	*Note	P0MD3	*Note	*Note	P0MD0
R	R	R	R	R/W	R	R	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0/1	0	0	0/1

* Note) Set always '0'.

3 Port 0 Output
0: P02 output
1: SBO0 I/O *

** Set bit 2 of PMSEL to '0'.*

0 Port 0 Output
0: P00 output
1: SBT0 I/O*

** Set bit 0 of PMSEL to '0'.*

P1MDA : x'00FFF2'

Port 1 Output Mode A Register

8/16-bit access register

7	6	5	4	3	2	1	0
*Note	P1MD A6	*Note	P1MD A4	*Note	P1MD A2	*Note	P1MD A0
R	R/W	R	R/W	R	R/W	R	R/W
0	0	0	0	0	0	0	0
0	0/1	0	0/1	0	0/1	0	0/1

* Note) Set always '0'.

6 Port 1 Output
0: P13 output
1: TM6IO output *

** Set bit 6 of PMSEL to '0'.*

4 Port 1 Output
0: P12 output
1: TM2IO output *

** Set bit 5 of PMSEL to '0'.*

2 Port 1 Output
0: P11 output
1: TM1IO output *

** Set bit 4 of PMSEL to '0'.*

0 Port 1 Output
0: P10 output
1: TM0IO output *

** Set bit 3 of PMSEL to '0'.*

P1MDB : x'00FFF3'

Port 1 Output Mode B Register

8-bit access register (16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
-	-	*Note	P1MD B4	*Note	P1MD B2	*Note	P1MD B0
R	R	R	R/W	R	R/W	R	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0	0/1	0	0/1

* Note) Set always '0'.

4 **Port 1 Output** 0: P16 output
1: TM9IO output

2 **Port 1 Output** 0: P15 output
1: TM8IO output

0 **Port 1 Output** 0: P14 output
1: TM7IO output *

** Set bit 7 of PMSEL to '0'.*

P3MD : x'00FFF4'

Port 3 Output Mode Register

8/16-bit access register

7	6	5	4	3	2	1	0
P3MD7	P3MD6	P3MD5	P3MD4	P3MD3	P3MD2	P3MD1	P3MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 **Port 3 Output** 0: P37 to P30 output
1: Inhibited

Set all to '0' always.

P

7	6	5	4	3	2	1	0
P4MD A7	P4MD A6	P4MD A5	P4MD A4	P4MD A3	P4MD A2	P4MD A1	P4MD A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P4MDA : x'00FFF6'

Port 4 Output Mode A Register

8/16-bit access register

7:6 Port 4 Output

00: P43 output
01: $\overline{\text{PWM1}}$ output
10: TM6IO output *
11: Inhibited

** Set bit 6 of PMSEL to '1'.*

5:4 Port 4 Output

00: P42 output
01: PWM1 output
10: TM2IO output *
11: Inhibited

** Set bit 5 of PMSEL to '1'.*

3:2 Port 4 Output

00: P41 output
01: $\overline{\text{PWM0}}$ output
10: TM1IO output *
11: Inhibited

** Set bit 4 of PMSEL to '1'.*

1:0 Port 4 Output

00: P40 output
01: PWM0 output
10: TM0IO output *
11: PWM0 output
(While $\overline{\text{NMI}}$ is generated, PWM2 to 0 and $\overline{\text{PWM2}}$ to 0 are prohibited to output.)

** Set bit 3 of PMSEL to '1'.*

P4MDB : x'00FFF7'

Port 4 Output Mode B Register

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
-	-	-	-	P4MD B3	P4MD B2	P4MD B1	P4MD B0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1

3:2 Port 4 Output

00: P45 output
01: PWM2 output
10: STOP output
11: Inhibited

1:0 Port 4 Output

00: P44 output
01: PWM2 output
10: TM7IO output *
11: Inhibited

** Set bit 7 of PMSEL to '1'.*

P5MD : x'00FFF8'

Port 5 Output Mode Register

8/16-bit access register

7	6	5	4	3	2	1	0
P5MD7	P5MD6	P5MD5	P5MD4	P5MD3	P5MD2	P5MD1	P5MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 5 Output

0: P57 to P50 output
1: Inhibited

Set all to '0' always.

P

7	6	5	4	3	2	1	0
P6MD A7	P6MD A6	P6MD A5	P6MD A4	P6MD A3	P6MD A2	P6MD A1	P6MD A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P6MDA : x'00FFFA'

Port 6 Output Mode A Register

8/16-bit access register

7 **Port 6 Output**
0: P64 output
1: TPWM4 output

6:5 **Port 6 Output**
00: P63 output
01: TPWM3 output
10: SBT1 I/O
11: Inhibited

4:3 **Port 6 Output**
00: P62 output
01: TPWM2 output
10: SBO0 I/O *
11: Inhibited

** Set bit 2 of PMSEL to '1'.*

2 **Port 6 Output**
0: P61 output
1: TPWM1 output

1:0 **Port 6 Output**
00: P60 output
01: TPWM0 output
10: SBT0 I/O *
11: Inhibited

** Set bit 0 of PMSEL to '1'.*

P6MDB : x'00FFFB'

Port 6 Output Mode B Register

8-bit access register
(16-bit access is possible from even address.)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	P6MD B1	P6MD B0
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1

1:0 Port 6 Output

00: P65 output
01: TPWM5 output
10: SBO1 I/O
11: Inhibited

P7MD : x'00FFFC'

Port 7 Output Mode Register

8/16-bit access register

7	6	5	4	3	2	1	0
*Note	P7MD6	*Note	*Note	*Note	*Note	*Note	P7MD0
R	R/W	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0
0	0/1	0	0	0	0	0	0/1

* Note) Set always '0'.

6 Port 7 Output

0: P77 output
1: $\overline{\text{WDOUT}}$ output

0 Port 7 Output

0: P70 output
1: BUZZ output

P

8-2-2 Control Register Address Map (1/2)

Upper 20 bits \ Lower 4 bits	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Remarks
x'00FC00'	IAGR ◆												MEMCTR ○		CPUM ○		Internal Control Register
x'00FC30'														SYSCTL	No Access See Note		System Control Register
x'00FC40'	G7ICR (VCT=14) ◆		G6ICR (VCT=12) ◆		G5ICR (VCT=10) ◆		G4ICR (VCT=8) ◆		G3ICR (VCT=6) ◆		G2ICR (VCT=4) ◆		G1ICR (VCT=2) ◆		G0ICR (VCT=0) ◆		Interrupt Control Register
x'00FC50'											WDREG ◆		NFCTR ◆		EXTMD ◆		
x'00FD00'															No Access See Note		
x'00FD70'													No Access See Note				
x'00FD80'									TXBUF0 *	RXBUF0 ◆		SC0CKS ◆	SC0MD3 *	SC0MD2 ◆	SC0MD1 *	SC0MD0 ◆	Serial Interface Channel 0
x'00FD90'									TXBUF1 *	RXBUF1 ◆		SC1CKS ◆	SC1MD3 *	SC1MD2 ◆	SC1MD1 *	SC1MD0 ◆	Serial Interface Channel 1
x'00FDB0'															ANCTR ◆		A/D Converter
x'00FDC0'	AN7BUF ○		AN6BUF ○		AN5BUF ○		AN4BUF ○		AN3BUF ○		AN2BUF ○		AN1BUF ○		AN0BUF ○		
x'00FE00'											TM5BC *	TM4BC ◆	TM3BC *	TM2BC ◆	TM1BC *	TM0BC ◆	Timer 12 Channels
x'00FE10'											TM5BR *	TM4BR ◆	TM3BR *	TM2BR ◆	TM1BR *	TM0BR ◆	
x'00FE20'											TM5MD *	TM4MD ◆	TM3MD *	TM2MD ◆	TM1MD *	TM0MD ◆	
x'00FE30'					TM6CBX ○		TM6CB ○		TM6CAX ○		TM6CA ○		TM6BC ○		TM6MD ○		
x'00FE40'					TM7CBX ○		TM7CB ○		TM7CAX ○		TM7CA ○		TM7BC ○		TM7MD ○		

◆ = 8/16-bit access ○ = 16-bit access * = 8-bit access (16-bit access is possible from an even address.) No symbol = 8-bit access

Note) x'00FC30', x'00FC31', x'00FD00', x'00FD01', x'00FD72' and x'00FD73' are the system reserve area. It is inhibited to access these addresses. If accessing them, the system operation cannot be guaranteed.

(2/2)

Upper 20 bits \ Lower 4 bits	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Remarks
x'00FE50'						TM8 CAX		TM8CB		TM8 CAX		TM8CA		TM8BC		TM8MD ○	Timer 12 Channels
x'00FE60'						TM9 CAX		TM9CB		TM9 CAX		TM9CA		TM9BC		TM9MD ○	
x'00FE70'						TM10 CAX		TM10CB		TM10 CAX		TM10CA		TM10BC		TM10MD ○	
x'00FE80'		TM11DT ○		TM11CC ○		TM11CB ○		TM11CA ○		TM11BR ○		TM11SL ○		TM11EX ○		TM11MD ○	
x'00FE90'																TM11CK ○	
x'00FFA0'														ANSEL ♦		PMSEL ♦	I/O Port
x'00FFB0'											PPDWB *	PPDWA ♦		PPUPC ♦	PPUPB *	PPUPA ♦	
x'00FFC0'									P7OUT *	P6OUT ♦	P5OUT *	P4OUT ♦	P3OUT *	P2OUT ♦	P1OUT *	P0OUT ♦	
x'00FFD0'									P7IN *	P6IN ♦	P5IN *	P4IN ♦	P3IN *	P2IN ♦	P1IN *	P0IN ♦	
x'00FFE0'									P7DIR *	P6DIR ♦	P5DIR *	P4DIR ♦	P3DIR *	P2DIR ♦	P1DIR *	P0DIR ♦	
x'00FFF0'				P7MD ♦	P6MDB *	P6MDA ♦		P5MD ♦	P4MDB *	P4MDA ♦		P3MD ♦	P1MDB *	P1MDA ♦		P0MD ♦	

♦ = 8/16-bit access ○ = 16-bit access * = 8-bit access (16-bit access is possible from an even address.) No symbol = 8-bit access

8-2-3 List of Pin Functions

EE = External excitation

	Pin name	Input Level	Output level	Schmitt trigger	Pull-up/down register	Reset	STOP/HALT
1	P70, BUZZ	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
2	P71	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
3	P72	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
4	P73	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
5	P74	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
6	P75	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
7	P76	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
8	P77, $\overline{\text{WDOUT}}$	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
9	V_{SS}	-	-	-	-	-	-
10	$\overline{\text{RST}}$	CMOS	-	Yes	Always	LOW input	High
11	V_{SS}	-	-	-	-	-	-
12	SYSCLK	-	CMOS	-	No	High	*1
13	V_{DD}	-	-	-	-	-	-
14	OSCI	-	-	-	-	-	-
15	OSCO	-	-	-	-	High (EE)	*1
16	V_{DD}	-	-	-	-	-	*
17	P50	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
18	P51	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
19	P52	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
20	P53	TTL	CMOS	No	Programmable (down)	Hi-Z	*
21	P54, AN11	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
22	P55, AN10	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
23	P56, AN9	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
24	P57, AN8	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
25	P30, AN7	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
26	P31, AN6	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
27	P32, AN5	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
28	P33, AN4	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
29	P34, AN3	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
30	P35, AN2	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
31	P36, AN1	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
32	P37, AN0	Analog/TTL	CMOS	No	Programmable (down)	Hi-Z	*
33	P00, SBT0	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
34	P01, SBI0	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
35	P02, SBO0	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
36	P10, TM0IO	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
37	P11, TM1IO	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
38	P12, TM2IO	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
39	P13, TM6IO	CMOS	CMOS	No	Programmable (up)	Hi-Z	*
40	P14, TM7IO	CMOS	CMOS	No	Programmable (up)	Hi-Z	*

41	P15, TM8IO	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
42	P16, TM9IO	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
43	P20, $\overline{\text{IRQ0}}$	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
44	P21, $\overline{\text{IRQ1}}$	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
45	P22, $\overline{\text{IRQ2}}$	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
46	P23, $\overline{\text{IRQ3}}$	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
47	P24, $\overline{\text{IRQ4}}$	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
48	P25, $\overline{\text{IRQ5}}$	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
49	V40, PWM0, TM0IO	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
50	P41, $\overline{\text{PWM0}}$, TM1IO	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
51	P42, PWM1, TM2IO	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
52	P43, $\overline{\text{PWM1}}$.,TM6IO	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
53	P44, PWM2, TM7IO	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
54	P45, $\overline{\text{PWM2}}$, STOP	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
55	P60, TPWM0, SBT0	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
56	P61, TPWM1, SBI0	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
57	P62, TPWM2, SBO0	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
58	P63, TPWM3, SBT1	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
59	P64, TPWM4, SBI1	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
60	P65, TPWM5, SBO1	CMOS	CMOS	Yes	Programmable (up)	Hi-Z	*
61	V_{DD}	-	-	-	-	-	-
62	PULUP	-	-	-	-	-	-
63	PULUP	-	-	-	-	-	-
64	$\overline{\text{NMI}}$	CMOS	-	Yes	No	$\overline{\text{NMI}}$	$\overline{\text{NMI}}$

*: Depends on pin setting. *1: High at STOP mode

8-3 MN10200 Series Linear Addressing Version Instructions

MN102 L00 SERIES INSTRUCTION SET

Instruction	Mnemonic	Operation	OP EX.	Flag VX	CX	NX	ZX	VF	CF	NF	ZF	Code Size	Cycle	Machine Code
MOV	MOV Dm, An	Dm → An	–	–	–	–	–	–	–	–	–	2	2	F2:30+Dm<<2+An
	MOV An, Dm	An → Dm	–	–	–	–	–	–	–	–	–	2	2	F2:F0+An<<2+Dm
	MOV Dn, Dm	Dn → Dm	–	–	–	–	–	–	–	–	–	1	1	80+Dn<<2+Dm ∗1
	MOV An, Am	An → Am	–	–	–	–	–	–	–	–	–	2	2	F2:70+An<<2+Am
	MOV PSW, Dn	PSW → Dn	0	–	–	–	–	–	–	–	–	2	2	F3:F0+Dn
	MOV Dn, PSW	Dn → PSW	–	●	●	●	●	●	●	●	●	2	3	F3:D0+Dn<<2
	MOV MDR, Dn	MDR → Dn	0	–	–	–	–	–	–	–	–	2	2	F3:E0+Dn
	MOV Dn, MDR	Dn → MDR	–	–	–	–	–	–	–	–	–	2	2	F3:C0+Dn<<2
	MOV (An), Dm	mem16 (An) → Dm	S	–	–	–	–	–	–	–	–	1	1	20+An<<2+Dm
	MOV (d8, An), Dm	mem16 (An+d8) → Dm	S	–	–	–	–	–	–	–	–	2	1	60+An<<2+Dm:d8
	MOV (d16, An), Dm	mem16 (An+d16) → Dm	S	–	–	–	–	–	–	–	–	4	2	F7:C0+An<<2+Dm:d16-l:d16-h
	MOV (d24, An), Dm	mem16 (An+d24) → Dm	S	–	–	–	–	–	–	–	–	5	3	F4:80+An<<2+Dm:d24-l:d24-m:d24-h
	MOV (Di, An), Dm	mem16 (An+Di) → Dm	S	–	–	–	–	–	–	–	–	2	2	F1:40+Di<<4+An<<2+Dm
	MOV (abs16), Dn	mem16 (abs16) → Dn	S	–	–	–	–	–	–	–	–	3	1	C8+Dn:abs16-l:abs16-h
	MOV (abs24), Dn	mem16 (abs24) → Dn	S	–	–	–	–	–	–	–	–	5	3	F4:C0+Dn:abs24-l:abs24-m:abs24-h
	MOV (An), Am	mem24 (An) → Am	–	–	–	–	–	–	–	–	–	2	2	∗2
	MOV (d8, An), Am	mem24 (An+d8) → Am	–	–	–	–	–	–	–	–	–	2	2	70+An<<2+Am:d8
	MOV (d16, An), Am	mem24 (An+d16) → Am	–	–	–	–	–	–	–	–	–	4	3	F7:B0+An<<2+Am:d16-l:d16-h
	MOV (d24, An), Am	mem24 (An+d24) → Am	–	–	–	–	–	–	–	–	–	5	4	F4:F0+An<<2+Am:d24-l:d24-m:d24-h
	MOV (Di, An), Am	mem24 (An+Di) → Am	–	–	–	–	–	–	–	–	–	2	3	F1:00+Di<<4+An<<2+Am
	MOV (abs16), An	mem24 (abs16) → An	–	–	–	–	–	–	–	–	–	4	3	F7:30+An:abs16-l:abs16-h
	MOV (abs24), An	mem24 (abs24) → An	–	–	–	–	–	–	–	–	–	5	4	F4:D0+An:abs24-l:abs24-m:d24-h
	MOV Dm, (An)	Dm → mem16 (An)	–	–	–	–	–	–	–	–	–	1	1	00+An<<2+Dm
	MOV Dm, (d8, An)	Dm → mem16 (An+d8)	–	–	–	–	–	–	–	–	–	2	1	40+An<<2+Dm:d8
	MOV Dm, (d16, An)	Dm → mem16 (An+d16)	–	–	–	–	–	–	–	–	–	4	2	F7:80+An<<2+Dm:d16-l:d16-h
	MOV Dm, (d24, An)	Dm → mem16 (An+24)	–	–	–	–	–	–	–	–	–	5	3	F4:00+An<<2+Dm:d24-l:d24-m:abs24-h
	MOV Dm, (Di, An)	Dm → mem16 (An+Di)	–	–	–	–	–	–	–	–	–	2	2	F1:C0+Di<<4+An<<2+Dm
	MOV Dn, (abs16)	Dm → mem16 (abs16)	–	–	–	–	–	–	–	–	–	3	1	C0+Dn:abs16-l:abs16-h
	MOV Dn, (abs24)	Dm → mem16 (abs24)	–	–	–	–	–	–	–	–	–	5	3	F4:40+Dn:abs24-l:abs24-m:abs24-h
	MOV Am, (An)	Am → mem24 (An)	–	–	–	–	–	–	–	–	–	2	2	∗3
	MOV Am, (d8, An)	Am → mem24 (An+d8)	–	–	–	–	–	–	–	–	–	2	2	50+An<<2+Am:d8
	MOV Am, (d16, An)	Am → mem24 (An+d16)	–	–	–	–	–	–	–	–	–	4	3	F7:A0+An<<2+Am:d16-l:d16-h
	MOV Am, (d24, An)	Am → mem24 (An+d24)	–	–	–	–	–	–	–	–	–	5	4	F4:10+An<<2+Am:d24-l:d24-m:d24-h
	MOV Am, (Di, An)	Am → mem24 (An+Di)	–	–	–	–	–	–	–	–	–	2	3	F1:80+Di<<4+An<<2+Am
	MOV An, (abs16)	Am → mem24 (abs16)	–	–	–	–	–	–	–	–	–	4	3	F7:20+An:abs16-l:abs16-h
	MOV An, (abs24)	Am → mem24 (abs24)	–	–	–	–	–	–	–	–	–	5	4	F4:50+An:abs24-l:abs24-m:abs24-h
	MOV imm8, Dn	imm8 → Dn	S	–	–	–	–	–	–	–	–	2	1	80+Dn<<2+Dn:imm8
	MOV imm16, Dn	imm16 → Dn	S	–	–	–	–	–	–	–	–	3	1	F8+Dn:imm16-l:imm16-h
	MOV imm24, Dn	imm24 → Dn	–	–	–	–	–	–	–	–	–	5	3	F4:70+Dn:imm24-l:imm24-m:imm24-h
	MOV imm16, An	imm16 → An	0	–	–	–	–	–	–	–	–	3	1	DC+An:imm16-l:imm16-h
	MOV imm24, An	imm24 → An	–	–	–	–	–	–	–	–	–	5	3	F4:74+An:imm24-l:imm24-m:imm24-h
MOVX	MOVX (d8, An), Dm	mem24 (An+d8) → Dm	–	–	–	–	–	–	–	–	–	3	3	F5:70+An<<2+Dm:d8
	MOVX (d16, An), Dm	mem24 (An+d16) → Dm	–	–	–	–	–	–	–	–	–	4	3	F7:70+An<<2+Dm:d16-l:d16-h
	MOVX (d24, An), Dm	mem24 (An+d24) → Dm	–	–	–	–	–	–	–	–	–	5	4	F4:B0+An<<2+Dm:d24-l:d24-m:d24-h
	MOVX Dm, (d8, An)	Dm → mem24 (An+d8)	–	–	–	–	–	–	–	–	–	3	3	F5:50+An<<2+Dm:d8
	MOVX Dm, (d16, An)	Dm → mem24 (An+d16)	–	–	–	–	–	–	–	–	–	4	3	F7:60+An<<2+Dm:d16-l:d16-h
	MOVX Dm, (d24, An)	Dm → mem24 (An+d24)	–	–	–	–	–	–	–	–	–	5	4	F4:30+An<<2+Dm:d24-l:d24-m:d24-h
MOVB	MOVB (An), Dm	mem8 (An) → Dm	S	–	–	–	–	–	–	–	–	2	2	∗4
	MOVB (d8, An), Dm	mem8 (An+d8) → Dm	S	–	–	–	–	–	–	–	–	3	2	F5:20+An<<2+Dm:d8
	MOVB (d16, An), Dm	mem8 (An+d16) → Dm	S	–	–	–	–	–	–	–	–	4	2	F7:D0+An<<2+Dm:d16-l:d16-h
	MOVB (d24, An), Dm	mem8 (An+d24) → Dm	S	–	–	–	–	–	–	–	–	5	3	F4:A0+An<<2+Dm:d24-l:d24-m:d24-h
	MOVB (Di, An), Dm	mem8 (An+Di) → Dm	S	–	–	–	–	–	–	–	–	2	2	F0:40+Di<<4+An<<2+Dm
	MOV (abs16), Dn	mem8 (abs16) → Dn	S	–	–	–	–	–	–	–	–	4	2	∗5
	MOVB (abs24), Dn	mem8 (abs24) → Dns	S	–	–	–	–	–	–	–	–	5	3	F4:C4+Dn:abs24-l:abs24-m:abs24-h
	MOVB Dm, (An)	Dm → mem8 (An)	–	–	–	–	–	–	–	–	–	1	1	10+Dm<<2+An
	MOVB Dm, (d8, An)	Dm → mem8 (An+d8)	–	–	–	–	–	–	–	–	–	3	2	F5:10+An<<2+Dm:d8
	MOVB Dm, (d16, An)	Dm → mem8 (An+d16)	–	–	–	–	–	–	–	–	–	4	2	F7:90+An<<2+Dm:d16-l:d16-h
	MOVB Dm, (d24, An)	Dm → mem8 (An+d24)	–	–	–	–	–	–	–	–	–	5	3	F4:20+An<<2+Dm:d24-l:d24-m:d24-h
	MOVB Dm, (Di, An)	Dm → mem8 (An+Di)	–	–	–	–	–	–	–	–	–	2	2	F0:C0+Di<<4+An<<2+Dm

Notes: ∗1 It is not possible to specify that Dn=Dm.
∗2 This instruction is supported by the aseembler. For "MOV (d8, An), Am" the assembler will generate a bit pattern d8=0.
∗3 This instruction is supported by the assembler. For "MOV Am, (d8, An)" the assembler will generate a bit pattern d8=0.
∗4 This instruction is supported by the assembler. The assembler generates bit patterns for the two instructions "MOVBU (An), Dm" and "EXTXB Dm".
∗5 This instruction is supported by the assembler. The assembler generates bit patterns for the two instructions "MOVBU (abs16), Dn" and "EXTXB Dn".

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
MOVB	MOVB Dn, (abs16)	Dm → mem8 (abs16)	-	-	-	-	-	-	-	-	-	3	1	C4+Dn:abs16-1:abs16-h
	MOVB Dn, (abs24)	Dm → mem8 (abs24)	-	-	-	-	-	-	-	-	-	5	3	F4:44+Dn:abs24-l:abs24-m:abs24-h
MOVBU	MOVBU (An), Dm	mem8 (An) → Dm	0	-	-	-	-	-	-	-	-	1	1	30+An<<2+Dm
	MOVBU (d8, An), Dm	mem8 (An+d8) → Dm	0	-	-	-	-	-	-	-	-	3	2	F5:30+An<<2+Dm:d8
	MOVBU (d16, An), Dm	mem8 (An+d16) → Dm	0	-	-	-	-	-	-	-	-	4	2	F7:50+An<<2+Dm:d16-l:d16-h
	MOVBU (d24, An), Dm	mem8 (An+d24) → Dm	0	-	-	-	-	-	-	-	-	5	3	F4:90+An<<2+Dm:d24-l:d24-m:d24-h
	MOVBU (Di, An), Dm	mem8 (An+Di) → Dm	0	-	-	-	-	-	-	-	-	2	2	F0:80+Di<<4+An<<2+Dm
	MOVBU (abs16), Dn	mem8 (abs16) → Dn	0	-	-	-	-	-	-	-	-	3	1	CC+Dn:abs16-l:abs16-h
	MOVBU (abs24), Dn	mem8 (abs24) → Dn	0	-	-	-	-	-	-	-	-	5	3	F4:C8+Dn:abs24-l:abs24-m:abs24-h
EXT	EXT Dn	If Dn.bp15=0, x'0000' → MDR If Dn.bp15=1, x'FFFF' → MDR	S	-	-	-	-	-	-	-	-	2	3	F3:C1+Dn<<2 *6
EXTX	EXTX Dn	If Dn.bp15=0, Dn&x'00FFFF' → Dn If Dn.bp15=1, Dn|x'FFFF' → Dn	S	-	-	-	-	-	-	-	-	1	1	B0+Dn *7
EXTXU	EXTXU Dn	Dn&x'00FFFF' → Dn	0	-	-	-	-	-	-	-	-	1	1	B4+Dn *8
EXTXB	EXTXB Dn	If Dn.bp7=0, Dn&x'0000FF' → Dn If Dn.bp7=1, Dn|x'FFFF00' → Dn	S	-	-	-	-	-	-	-	-	1	1	B8+Dn *9
EXTXBU	EXTXBU Dn	Dn&x'0000FF → Dn	0	-	-	-	-	-	-	-	-	1	1	BC+Dn *10
ADD	ADD Dn, Dm	Dm+Dn → Dm	-	●	●	●	●	●	●	●	●	1	1	90+Dn<<2+Dm
	ADD Dm, An	An+Dm → An	-	●	●	●	●	●	●	●	●	2	2	F2:Dm<<2+An
	ADD An, Dm	Dm+An → Dm	-	●	●	●	●	●	●	●	●	2	2	F2:C0+An<<2+Dm
	ADD An, Am	Am+An → Am	-	●	●	●	●	●	●	●	●	2	2	F2:40+An<<2+Am
	ADD imm8, Dn	Dn+imm8 → Dn	S	●	●	●	●	●	●	●	●	2	1	D4+Dn:imm8
	ADD imm16, Dn	Dn+imm16 → Dn	S	●	●	●	●	●	●	●	●	4	2	F7:18+Dn:imm16-l:imm16-h
	ADD imm24, Dn	Dn+imm24 → Dn	-	●	●	●	●	●	●	●	●	5	3	D4:60+Dn:imm24-l:imm24-m:imm24-h
	ADD imm8, An	An+imm8 → An	S	●	●	●	●	●	●	●	●	2	1	D0+An:imm8 *11
	ADD imm16, An	An+imm16 → An	S	●	●	●	●	●	●	●	●	4	2	F7:08+An:imm16-l:imm16-h
	ADD imm24, An	An+imm24 → An	-	●	●	●	●	●	●	●	●	5	3	F4:64+An:imm24-l:imm24-m:imm24-h
ADDC	ADDC Dn, Dm	Dm+Dn+CF → Dm	-	●	●	●	●	●	●	●	●	2	2	F2:80+Dn<<2+Dm
ADDNF	ADDNF imm8, An	An+imm8 → An	S	-	-	-	-	-	-	-	-	3	2	F5:0C+An:imm8
SUB	SUB Dn, Dm	Dm-Dn → Dm	-	●	●	●	●	●	●	●	●	1	1	A0+Dn<<2+An
	SUB Dm, An	An-Dm → An	-	●	●	●	●	●	●	●	●	2	2	F2:10+Dn<<2+An
	SUB An, Dm	Dm-An → Dm	-	●	●	●	●	●	●	●	●	2	2	F2:D0+An<<2+Dm
	SUB An, Am	Am-An → Am	-	●	●	●	●	●	●	●	●	2	2	F2:50+An<<2+Am
	SUB imm16, Dn	Dn-imm16 → Dn	S	●	●	●	●	●	●	●	●	4	2	F7:1C+Dn:imm16-l:imm16-h
	SUB imm24, Dn	Dn-imm24 → Dn	-	●	●	●	●	●	●	●	●	5	3	F4:68+Dn:imm24-l:imm24-m:imm24-h
	SUB imm16, An	An-imm16 → An	S	●	●	●	●	●	●	●	●	4	2	F7:0C+An:imm16-l:imm16-h
	SUB imm24, An	An-imm24 → An	-	●	●	●	●	●	●	●	●	5	3	F4:6C+An:imm24-l:imm24-m:imm24-h
SUBC	SUBC Dn, Dm	Dm-Dn → Dm	-	●	●	●	●	●	●	●	●	2	2	F2:90+Dn<<2+Dm
MUL	MUL Dn, Dm	Dm*Dn → Dm (Dm*Dn)>>16 → MDR	-	?	?	?	?	0	?	●	●	2	12	F3:40+Dn<<2+Dm *12
MULU	MULU Dn, Dm	Dm*Dn → Dm (Dm*Dn)>>16 → MDR	-	?	?	?	?	0	?	●	●	2	12	F3:50+Dn<<2+Dm *13
DIVU	DIVU Dn, Dm	(MDR<<16+Dm)Dn → Dm ...MDR	-	?	?	●/?	●/?	0/1	?	●/?	●/?	2	13	F3:60+Dn<<2+Dm *14

Notes: *6 32-bit sign extended word data
*7 24-bit sign extended word data
*8 24-bit zero extended word data
*9 24-bit sign extended byte data
*10 24-bit zero extended byte data
*11 Addition without changing flag
*12 16 × 16=32 (signed)
*13 16 × 16=32 (unsigned)
*14 32 ÷ 16=16...16 (unsigned)

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
CMP	CMP Dn, Dm	Dm-Dn	-	●	●	●	●	●	●	●	●	2	2	F3:90+Dn<<2+Dm
	CMP Dm, An	An-Dm	-	●	●	●	●	●	●	●	●	2	2	D2:20+Dm<<2+An
	CMP An, Dm	Dm-An	-	●	●	●	●	●	●	●	●	2	2	F2+E0+An<<2+Dm
	CMP An, Am	Am-An	-	●	●	●	●	●	●	●	●	2	2	F2:60+An<<2+Am
	CMP imm8, Dn	Dn-imm8	S	●	●	●	●	●	●	●	●	2	1	D8+Dn:imm8
	CMP imm16, Dn	Dn-imm16	S	●	●	●	●	●	●	●	●	4	2	F7:48+Dn:imm16-l:imm16-h
	CMP imm24, Dn	Dn-imm24	-	●	●	●	●	●	●	●	●	5	3	F4:78+Dn:imm24-l:imm24-m:imm24-h
	CMP imm16, An	An-imm16	0	●	●	●	●	●	●	●	●	3	1	EC+An:imm16-l:imm16-h
	CMP imm24, An	An-imm24	-	●	●	●	●	●	●	●	●	5	3	F4:7C+An:imm24-l:imm24-m:imm24-h
AND	AND Dn, Dm	Dm&(x'FF0000'|Dn') → Dm	-	-	-	-	-	0	0	●	●	2	2	F3:00+Dn<<2+Dm *15
	AND imm8, Dn	Dn&(x'FF0000'|imm8) → Dn	0	-	-	-	-	0	0	●	●	3	2	F5:00+Dn:imm8 *15
	AND imm16, Dn	Dn&(x'FF0000'|imm16) → Dn	-	-	-	-	-	0	0	●	●	4	2	F7:00+Dn:imm16-l:imm16-h *15
	AND imm16, PSW	PSW&imm16 → PSW	-	●	●	●	●	●	●	●	●	4	3	F7:10:imm16-l:imm16-h *15
OR	OR Dn, Dm	Dm|(Dn&x'00FFFF') → Dm	-	-	-	-	-	0	0	●	●	2	2	F3:10+Dn<<2+Dm *15
	OR imm8, Dn	Dn|imm8 → Dn	0	-	-	-	-	0	0	●	●	3	2	F5:08+Dn:imm8 *15
	OR imm16, Dn	Dn|imm16 → Dn	-	-	-	-	-	0	0	●	●	4	2	D7:40+Dn:imm16-l:imm16-h *15
	OR imm16, PSW	PSW|imm16 → PSW	-	●	●	●	●	●	●	●	●	4	3	F7:14:imm16-l:imm16-h *15
XOR	XOR Dn, Dm	Dm^(x'00FFFF'&Dn) → Dm	-	-	-	-	-	0	0	●	●	2	2	F3:20+Dn<<2+Dm *15
	XOR imm16, Dn	Dn^imm16 → Dn	-	-	-	-	-	0	0	●	●	4	2	D7:4C+Dn:imm16-l:imm16-h *15
NOT	NOT Dn	Dn^x'00FFFF' → Dn	-	-	-	-	-	0	0	●	●	2	2	F3:E4+Dn *15
ASR	ASR Dn	Dn.lsb → CF Dn.bp → Dn.bp-1 (bp15 to 1) Dn.bp15 → Dn.bp15	-	-	-	-	-	0	●	●	●	2	2	F3:38+Dn *15
LSR	LSR Dn	Dn.lsb → CF Dn.bp → Dn.bp-1 (bp15 to 1) 0 → Dn.bp15	-	-	-	-	-	0	●	0	●	2	2	F3:3C+Dn *15
ROR	ROR Dn	Dn.lsb → temp Dn.bp → Dn.bp-1 (bp15 to 1) CF → Dn.bp15 temp → CF	-	-	-	-	-	0	●	●	●	2	2	F3:34+Dn *15
ROL	ROL Dn	Dn.bp15 → temp Dn.bp → Dn.bp+1 (bp14 to 0) CF → Dn.lsb temp → CF	-	-	-	-	-	0	●	●	●	2	2	F3:30+Dn *15
BTST	BTST imm8, Dn	Dn&imm8...PSW	0	-	-	-	-	0	0	0	●	3	2	F5:04+Dn:imm8
	BTST imm16, Dn	Dn&imm16...PSW	0	-	-	-	-	0	0	●	●	4	2	F7:04+Dn:imm16-l:imm16-h
BSET	BSET Dm, (An)	mem8(An)&Dm...PSW mem8(An)|Dm → mem8(An)	0	-	-	-	-	0	0	0	●	2	5	F0:20+An<<2+Dm *16
BCLR	BCLR Dm, (An)	mem8(An)&Dm...PSW mem8(An)&(~Dm → mem8(An)	0	-	-	-	-	0	0	0	●	2	5	F0:30+An<<2+Dm *16
Bcc	BEQ label	If ZF=1, PC+2+d8(label) → PC If ZF=0, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E8:d8 *17
	BNE label	If ZF=0, PC+2+d8(label) → PC If ZF=1, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E9:d8 *18
	BLT label	If (VF^NF)=1, PC+2+d8(label) → PC If (VF^NF)=0, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E0:d8 *19

Notes: *15 16-bit computation
*16 Performed under the condition of bus lock and disabled interrupt.
*17 src=dest (lower 16 bits)
*18 src≠dest (lower 16 bits)
*19 src>dest (lower 16 bits, signed)

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
Bcc	BLE label	If ((VF^NF)|ZF)=1, PC+2+d8(label) → PC If ((VF^NF)|ZF)=0, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E3:d8 *20
	BGE label	If (VF^NF)=0, PC+2+d8(label) → PC If (VF^NF)=1, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E2:d8 *21
	BGT label	If ((VF^NF)|ZF)=0, PC+2+d8(label) → PC If ((VF^NF)|ZF)=1, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E1:d8 *22
	BCS label	If CF=1, PC+2+d8(label) → PC If CF=0, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E4:d8 *23
	BLS label	If (CF|ZF)=1, PC+2+d8(label) → PC If (CF|ZF)=0, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E7:d8 *24
	BCC label	If CF=0, PC+2+d8(label) → PC If CF=1, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E6:d8 *25
	BHI label	If (CF|ZF)=0, PC+2+d8(label) → PC If (CF|ZF)=1, PC+2 → PC	-	-	-	-	-	-	-	-	-	2	2/1	E5:d8 *26
	BVC label	If VF=0, PC+3+d8(label) → PC If VF=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	E5:FC:d8 *27
	BVS label	If VF=1, PC+3+d8(label) → PC If VF=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	E5:FD:d8 *28
	BNC label	If NF=0, PC+3+d8(label) → PC If NF=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	E5:FE:d8 *29
	BNS label	If NF=1, PC+3+d8(label) → PC If NF=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	E5:FF:d8 *30
	BRA label	PC+2+d8(label) → PC	-	-	-	-	-	-	-	-	-	2	2	EA:d8
Bccx	BEQX label	If ZX=1, PC+3+d8(label) → PC If ZX=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	E5:E8:d8 *31
	BNEX label	If ZX=0, PC+3+d8(label) → PC If ZX=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	E5:E9:d8 *32

Notes: *20 src≥dest (lower 16 bits, signed)
*21 src≤dest (lower 16 bits, signed)
*22 src<dest (lower 16 bits, signed)
*23 src>dest (lower 16 bits, unsigned)
*24 src≥dest (lower 16 bits, unsigned)
*25 src≤dest (lower 16 bits, unsigned)
*26 src<dest (lower 16 bits, unsigned)
*27 VF=0
*28 VF=1
*29 NF=0
*30 NF=1
*31 src=dest (24 bits)
*32 src≠dest (24 bits)

Instruction	Mnemonic	Operation	OP EX.	Flag									Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF				
Bccx	BLTX label	If (VX^NX)=1, PC+3+d8(label) → PC If (VX^NX)=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:E0:d8 *33
	BLEX label	If ((VX^NX)|ZX)=1, PC+3+d8(label) → PC If ((VX^NX)|ZX)=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:E3:d8 *34
	BGEX label	If (VX^NX)=0, PC+3+d8(label) → PC If (VX^NX)=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:E2:d8 *35
	BGTX label	If ((VX^NX)|ZX)=0, PC+3+d8(label) → PC If ((VX^NX)|ZX)=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:E1:d8 *36
	BCSX label	If CX=1, PC+3+d8(label) → PC If CX=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:E4:d8 *37
	BLSX label	If (CX|ZX)=1, PC+3+d8(label) → PC If (CX|ZX)=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:E7:d8 *38
	BCCX label	If CX=0, PC+3+d8(label) → PC If CX=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:E6:d8 *39
	BHIX label	If (CX|ZX)=0, PC+3+d8(label) → PC If (CX|ZX)=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:E5:d8 *40
	BVCX label	If VX=0, PC+3+d8(label) → PC If VX=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:EC:d8 *41
	BVSX label	If VX=1, PC+3+d8(label) → PC If VX=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:ED:d8 *42
	BNCX label	If NX=0, PC+3+d8(label) → PC If NX=1, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:EE:d8 *43
	BNSX label	If NX=1, PC+3+d8(label) → PC If NX=0, PC+3 → PC	-	-	-	-	-	-	-	-	-	3	3/2	F5:EF:d8 *44
JMP	JMP label16	PC+3+d16(label16) → PC	-	-	-	-	-	-	-	-	-	3	2	FC:d16-l:d16-h
	JMP label24	PC+5+d24(label24) → PC	-	-	-	-	-	-	-	-	-	5	4	F4:E0:d24-l:d24-m:d24-h
	JMP (An)	An → PC	-	-	-	-	-	-	-	-	-	2	3	F0:An<<2

Notes: *33 src>dest (24 bits, signed)
*34 src≥dest (24 bits, signed)
*35 src≤dest (24 bits, signed)
*36 src<dest (24 bits, signed)
*37 src>dest (24 bits, unsigned)
*38 src≥dest (24bits, unsigned)
*39 src≤dest (24 bits, unsigned)
*40 src<dest (24 bits, unsigned)
*41 VX=0
*42 VX=1
*43 NX=0
*44 NX=1

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
JSR	JSR label16	A3-4 → A3 PC+3 → mem24 (A3) PC+3+d16 (label16) → PC	-	-	-	-	-	-	-	-	-	3	4	FD:d16-l:d16-h
	JSR label24	A3-4 → A3 PC+5 → mem24 (A3) PC+5+d24 (label24) → PC	-	-	-	-	-	-	-	-	-	5	5	F4:E1:d24-l:d24-m:d24-h
	JSR (An)	A3-4 → A3 PC+2 → mem24 (A3) An → PC	-	-	-	-	-	-	-	-	-	2	5	F0:01+An<<2
NOP	NOP	PC+1 → PC	-	-	-	-	-	-	-	-	-	1	1	F6
RTS	RTS	mem24 (A3) → PC A3+4 → A3	-	-	-	-	-	-	-	-	-	1	5	FE
RTI	RTI	mem16 (A3) → PSW mem16 (A3+2) → PC A3+6 → A3	-	●	●	●	●	●	●	●	●	1	6	EB

How to Read INSTRUCTION SET

■ Expression of symbols used in the chart

Dn, Dm, Di	Data register
An, Am	Address register
MDR, PSW, PC	Multiplications and division register, program status word, program counter
imm8, imm16, imm16-l, imm16-h	Constant
imm24, imm24-l, imm24-m, imm24-h	
d8, d16, d16-l, d16-h	Displacement
d24, d24-l, d24-m, d24-h	
abs16, abs16-l, abs16-h	Absolute address
abs24, abs24-l, abs24-m, abs24-h	
mem8 (An), mem8 (abs16), mem8 (abs24)	8-bit memory data referred at the address enclosed in parenthesis
mem16 (An), mem16 (abs16), mem16 (abs24)	16-bit memory data referred at the address enclosed in parenthesis
mem24 (Am), mem24 (abs16), mem24 (abs24)	24-bit memory data referred at the address enclosed in parenthesis
.bp, .lsb, .msb	Bit specification
&, |, ^	Logical AND, logical OR, exclusive OR
, <<	Bit reversal, bit shift
VX, CX, NX, ZX,	Extended overflow flag, extended carry flag, extended negative flag, extended zero flag
VF, CF, NF, ZF	Overflow flag, carry flag, negative flag, zero flag
temp	Temporary register inside of CPU
→, ...	Assignment, reflection of computation result

■ OP EX. (Operand Extension)

0 zero extension
S sign extension
- not applicable

■ Flag

● change
- no change
0 normally 0
1 normally 1
? undefined

■ Code Size

Unit: byte

■ Cycle

The minimum number of cycles are specified.
Unit: machine cycle
a/b : There are branches in the 'a' cycle.
There are no branches in the 'b' cycle.

■ Machine code

[:] separates the byte unit. [<<2] indicates a 2-bit shift.
Dn, Dm, Di, An, Am: register numbers

D0	00	A0	00
D1	01	A1	01
D2	10	A2	10
D3	11	A3	11

■ Notes

- Instructions that access 16-bit data and 24-bit data must use an even memory address.
- All 8-bit displacement (d8) and 16-bit displacement (d16) are sign extended.

MN102L00 SERIES INSTRUCTION MAP

First Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV Dm, (An)															
1	MOVB Dm, (An)															
2	MOV (An), Dm															
3	MOVBU (An), Dm															
4	MOV Dm, (d8, An)															
5	MOV Am (d8, An)															
6	MOV (d8, An), Dm															
7	MOV (d8, An), Am															
8	MOV Dn, Dm (When src=dest, MOV imm8, Dn)															
9	ADD Dn, Dm															
A	SUB Dn, Dm															
B	EXTX Dn				EXTXU Dn				EXTXB Dn				EXTXBU Dn			
C	MOV Dn, (abs16)				MOVB Dn, (abs16)				MOV (abs16), Dn				MOVBU (abs16), Dn			
D	ADD imm8, An				ADD imm8, Dn				CMP imm8, Dn				MOV imm16, An			
E	BLT label	BGT label	BGE label	BLE label	BCS label	BHI label	BCC label	BLS label	BEQ label	BNE label	BRA label	RTI	CMP imm16, An			
F	Code extended (2 bytes)				Code extended (5 bytes)	Code extended (3 bytes)	NOP	Code extended (4 bytes)	MOV imm16, Dn				JMP label16	JSR label16	RTS	

Two-Byte Instructions (First byte: F0)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP (A0)	JSR (A0)			JMP (A1)	JSR (A1)			JMP (A2)	JSR (A2)			JMP (A3)	JSR (A3)		
1																
2	BSET Dm, (An)															
3	BCLR Dm, (An)															
4–7	MOVB (Di, An), Dm															
8–B	MOVBU (Di, An), Dm															
C–F	MOVB Dm, (Di, An)															

Two-Byte Instructions (First byte: F1)

<table>
<tr><th>Second Byte Upper/Lower</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>F</th></tr>
<tr><td>0</td><td colspan="16" rowspan="4">MOV (Di, An), Am</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td><td colspan="16" rowspan="4">MOV (Di, An), Dm</td></tr>
<tr><td>5</td></tr>
<tr><td>6</td></tr>
<tr><td>7</td></tr>
<tr><td>8</td><td colspan="16" rowspan="4">MOV Am, (Di, An)</td></tr>
<tr><td>9</td></tr>
<tr><td>A</td></tr>
<tr><td>B</td></tr>
<tr><td>C</td><td colspan="16" rowspan="4">MOV Dm, (Di, An)</td></tr>
<tr><td>D</td></tr>
<tr><td>E</td></tr>
<tr><td>F</td></tr>
</table>

Two-Byte Instructions (First byte: F2)

<table>
<tr><th>Second Byte Upper/Lower</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>F</th></tr>
<tr><td>0</td><td colspan="16">ADD Dm, An</td></tr>
<tr><td>1</td><td colspan="16">SUB Dm, An</td></tr>
<tr><td>2</td><td colspan="16">CMP Dm, An</td></tr>
<tr><td>3</td><td colspan="16">MOV Dm, An</td></tr>
<tr><td>4</td><td colspan="16">ADD An, Am</td></tr>
<tr><td>5</td><td colspan="16">SUB An, Am</td></tr>
<tr><td>6</td><td colspan="16">CMP An, Am</td></tr>
<tr><td>7</td><td colspan="16">MOV An, Am</td></tr>
<tr><td>8</td><td colspan="16">ADDC Dn, Dm</td></tr>
<tr><td>9</td><td colspan="16">SUBC Dn, Dm</td></tr>
<tr><td>A</td><td colspan="16"></td></tr>
<tr><td>B</td><td colspan="16"></td></tr>
<tr><td>C</td><td colspan="16">ADD An, Dm</td></tr>
<tr><td>D</td><td colspan="16">SUB An, Dm</td></tr>
<tr><td>E</td><td colspan="16">CMP An, Dm</td></tr>
<tr><td>F</td><td colspan="16">MOV An, Dm</td></tr>
</table>

Two-Byte Instructions (First byte: F3)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND Dn, Dm															
1	OR Dn, Dm															
2	XOR Dn, Dm															
3	ROL Dn				ROR Dn				ASR Dn				LSR Dn			
4	MUL Dn, Dm															
5	MULU Dn, Dm															
6	DIVU Dn, Dm															
7																
8																
9	CMP Dn, Dm															
A																
B																
C	MOV D0, MDR	EXT D0			MOV D1, MDR	EXT D1			MOV D2, MDR	EXT D2			MOV D3, MDR	EXT D3		
D	MOV D0, PSW				MOV D1, PSW				MOV D2, PSW				MOV D3, PSW			
E	MOV MDR, Dn				NOT Dn											
F	MOV PSW, Dn															

Five-Byte Instructions (First byte: F4)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV Dm, (d24, An)															
1	MOV Am, (d24, An)															
2	MOVB Dm, (d24, An)															
3	MOVX Dm, (d24, An)															
4	MOV Dn, (abs24)				MOVB Dn, (abs24)											
5	MOV An, (abs24)															
6	ADD imm24, Dn				ADD imm24, An				SUB imm24, Dn				SUB imm24, An			
7	MOV imm24, Dn				MOV imm24, An				CMP imm24, Dn				CMP imm24, An			
8	MOV (d24, An), Dm															
9	MOVBU (d24, An), Dm															
A	MOVB (d24, An), Dm															
B	MOVX (d24, An), Dm															
C	MOV (abs24), Dn				MOVB (abs24), Dn				MOVBU (abs24), Dn							
D	MOV (abs24), An															
E	JMP label24	JSR label24														
F	MOV (d24, An), Am															

Three-Byte Instructions (First byte: F5)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND imm8, Dn				BTST imm8, Dn				OR imm8, Dn				ADDNF imm8, An			
1	MOVB Dm, (d8, An)															
2	MOVB (d8, An), Dm															
3	MOVBU (d8, An), Dm															
4																
5	MOVX Dm, (d8, An)															
6																
7	MOVX (d8, An), Dm															
8																
9																
A																
B																
C																
D																
E	BLTX label	BGTX label	BGEX label	BLEX label	BCSX label	BHIX label	BCCX label	BLSX label	BEQX label	BNEX label			BVCX label	BVSX label	BNCX label	BNSX label
F													BVC label	BVS label	BNC label	BNS label

Four-Byte Instructions (First byte: F7)

Second Byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND imm16, Dn				BTST imm16, Dn				ADD imm16, An				SUB imm16, An			
1	AND imm16 PSW				OR imm16 PSW				ADD imm16, Dn				SUB imm16, Dn			
2	MOV An, (abs16)															
3	MOV (abs16), An															
4	OR imm16, Dn								CMP imm16, Dn				XOR imm16, Dn			
5	MOVBU (d16, An), Dm															
6	MOVX Dm,(d16, An)															
7	MOVX (d16, An), Dm															
8	MOV Dm,(d16, An)															
9	MOVB Dm,(d16, An)															
A	MOV Am,(d16, An)															
B	MOV (d16, An), Am															
C	MOV (d16, An), Dm															
D	MOVB (d16, An), Dm															
E																
F																

8-4 Flash EEPROM Version

8-4-1 Overview

The MN102LF59D replaces the MN102L59X mask ROM with the 64-KB flash EEPROM which is an electrically programmable/erasable memory.

The MN102LF59D has two modes: PROM programming mode which uses a dedicated writer (a DATA-I/O LabSite writer) and onboard serial programming mode which uses the CPU controls.

The 64-KB flash memory is divided into two areas as follows:

1. Load program area (6 KB: x'80000' to x'817FF')
   This area stores the load program for serial programming.
   It is used only in PROM programming mode.

2. Firm area (58 KB: x'81800' to x'8FFFF')
   This area stores the user program.
   It can be programmed in PROM writer/onboard serial programming mode.

> **!** 1 cycle of “erase → program” is counted as one of programming regardless of areas. Even if programming a certain area only one time, when multiple areas are programmed separately, a number of programming is added.
> Programming multiple areas should be done at a time to reduce the number of programming.

8-4-2 Flash EEPROM Programming

The following figure shows the steps of flash memory programming (erase/write).

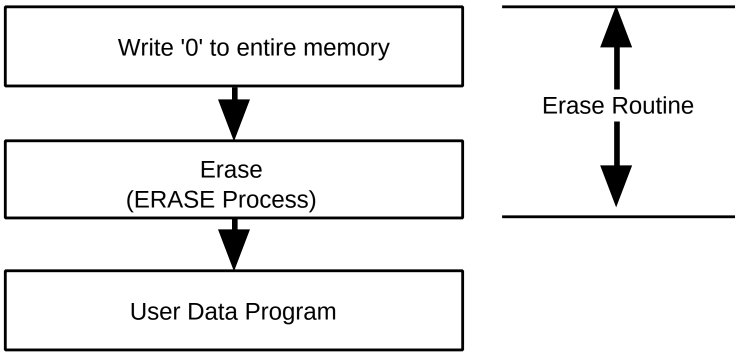

Figure 8-4-1 Flash EEPROM Program Flow

As the above figure shows, programming starts after erasing is completed. The whole erase routine consists of two steps:

1. Programming process which writes x’0000' to flash EEPROM before the actual erase process occurs
2. Erase process which operates the actual erasing

8-4-3 PROM Programming Mode

In this mode, the MN102LF59D allows a PROM writer to program the flash EEPROM.

The MN102LF59D uses a dedicated writing adaptor, which connects to the DATA-I/O's LabSite PROM writer. (Using the dedicated writing adaptor selects PROM programming mode automatically.)

8-4-4 Onboard Serial Programming Mode

The serial programming mode is used to program the flash ROM in the MN102LF59D that is installed on the board by using CPU.
The following sections describe the MN102LF59D hardware, system configuration and protocol for this programming mode.

When using YDC dedicated writer, please follow its user manual. The load program is attached to the serial writer.

8-4-5 Hardware Used in Serial Programming Mode

(1) Interface
The MN102LF59D has the following functions as interface for serial programming.

- One 8-bit Serial Interface
    - Data transmission/reception synchronizing external clock
    - Bit order: LSB first
    - Maximum clock speed: 10 MHz
    - Positive input/output logic

- Two Input/Output Pins
    - SBT and SBD reserved for serial interface

(2) Interface Block Diagram

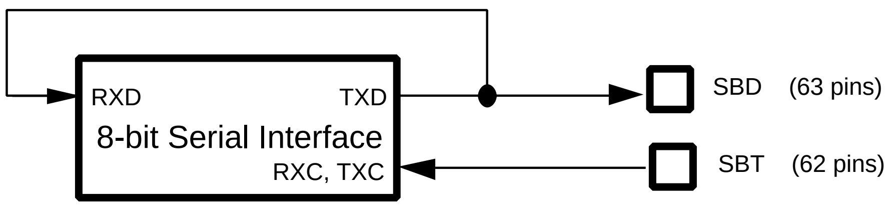

Figure 8-4-2 8-bit Serial Interface Block Diagram for Serial Writer

(3) Memory Space of Internal Flash EEPROM

Address	Size	Contents
0x80000 | 0x817FF	6 KB	Serial writer Load storage space
0x81800 | 0x81807	8 Bytes	Reserved space
0x81808	8 Bytes	Branch instruction to reset start service routine
0x81810	8 Bytes	Branch instruction to interrupt service routine
0x81818 | 0x8FFFF	57 KB	User program space

Table 8-4-1 Flash EEPROM Memory Space

- Serial Writer Load Storage Space
  - The 6-KB space from x'80000' stores the load program for serial writer.
  - In onboard serial programming mode, the erasing/programming in this space is protected. (Programming is possible by using the parallel writer.)

- Branch Instruction to Reset Start Service Routine
  - The reset start address is normally x'80000', but the program branches into x'81808' with the soft branch instruction in the serial writer loader. In this area, the JMP instruction to the actual reset service routine is stored.

- Branch Instruction to Interrupt Service Routine
  - The jump address at interrupt is normally x'80008', but the program branches into x'81810' with the soft branch instruction in the serial writer loader. In this area, the JMP instruction to the actual interrupt service routine is stored.

- User Program Space
  - This space stores the user program.

8-4-6 Connecting at Onboard Serial Programming Mode

Use YDC serial writer for flash microcontroller.
All input/output pins must be set to input at reset release.

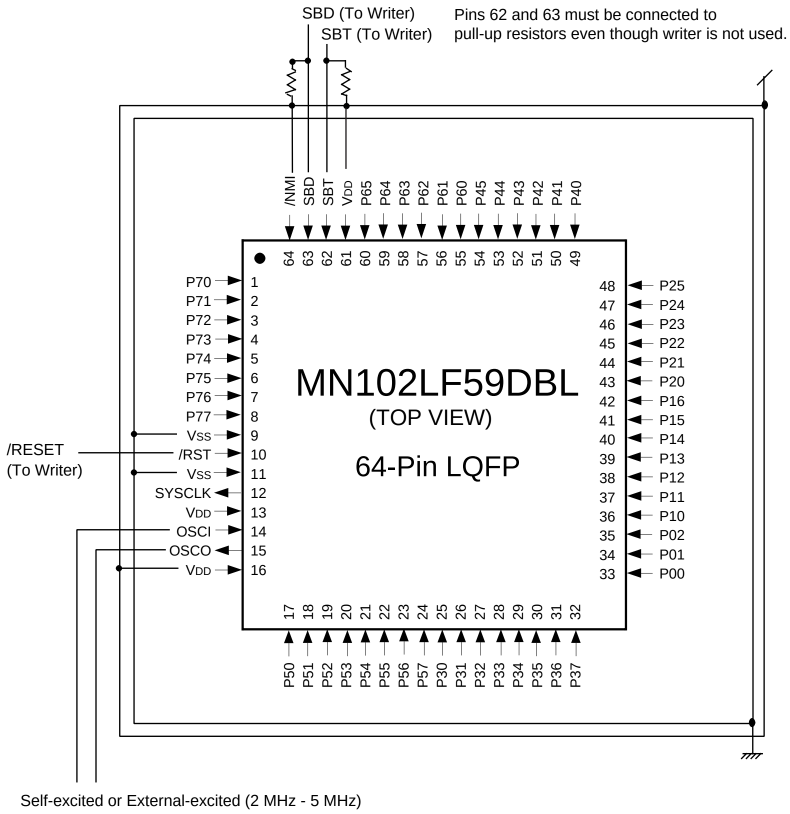

Figure 8-4-3 Pin Configuration During Serial Programming

Switch the connection of pins 10, 62 and 63 to the serial writer.
Connect VDD and Vss to the external power sources of 5 V and 0 V respectively.
In addition, the level is detected by the writer, VDD and Vss must be output to the writer also.
OSCI and OSCO must be set to the self-excited oscillation or external excited oscillation.
The input pins with no specifications in the above figure are 'don't care'. Fix them to VDD or Vss.
The output pins with no specifications in the above figure must be open.

8-4-7 System Configuration at Onboard Serial Programming

(1) System Configuration

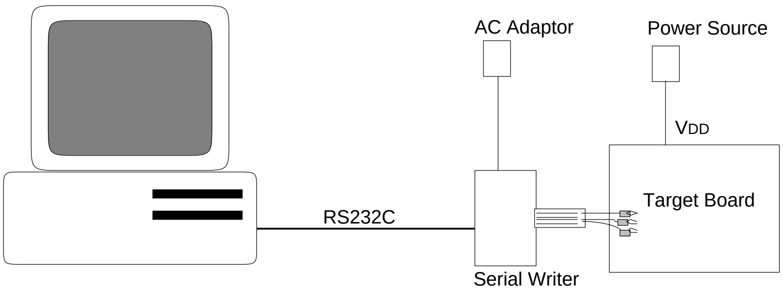

Figure 8-4-4 System Configuration for Onboard Serial Writer

- The PC sends the program data to the serial writer through RS-232C.
- The serial writer programs the flash memory through serial communication between the serial writer and the MN102L59D on the target board.
- The power is required only when the power source is supplied to the target.

(2) Pin Connection for Target Board

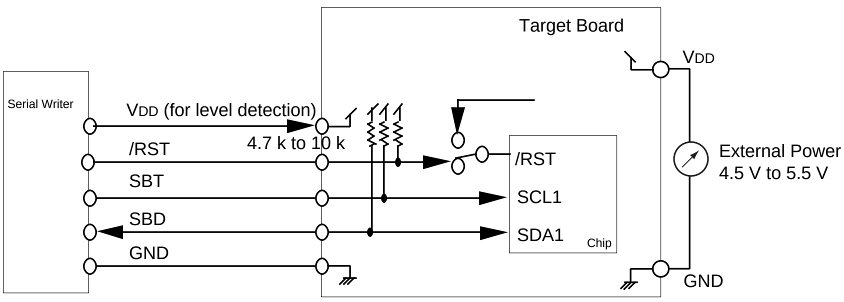

Figure 8-4-5 Target Board-Serial Writer Connection

(3) Pin Description

- VDD : 4.5 V to 5.5 V external power supply
- VDD (for level detection) : VDD level detection pin for target board
- /RST : Reset
- SBT : Serial interface clock supply
- SBD : Serial interface data supply
- GND : Ground

- /RST outputs microcontroller reset.
- Connect pull-up resistors to /RST, SBT and SBD on the target board. The pull-up resistor value is 4.7 kΩ ± 10 % to 10 kΩ ± 10 %.
- /RST, SBT and SBD are output from the serial writer through an open collector.

(4) MN102LF59D Clock on the Target Board

- Use the existing clock on the target board for the clock supply to the MN102LF59D on the target board. Because of this, the clock frequency of the MN102LF59D differs depending on each user purpose.
- The following table shows the clock frequency for the MN102LF59D during serial programming. The clock frequency for the MN102LF59D is assumed to be 5 MHz if it is not specified in the manual. If the clock frequency for the MN102LF59D is different from one on the target board, the value should be calculated proportionately depending on the clock frequency of the MN102LF59D.

Table 8-4-2 Clock Frequency

Max. Clock Frequency	Min. Clock Frequency
5 MHz (Internal: 20 MHz)	2 MHz (Internal: 8 MHz)

8-4-8 Onboard Serial Programming Mode Setup

(1) Programming Mode Setup Timing

To set serial programming mode, the microcontroller must be in write mode.
This section describes the pin setup for the serial writer.

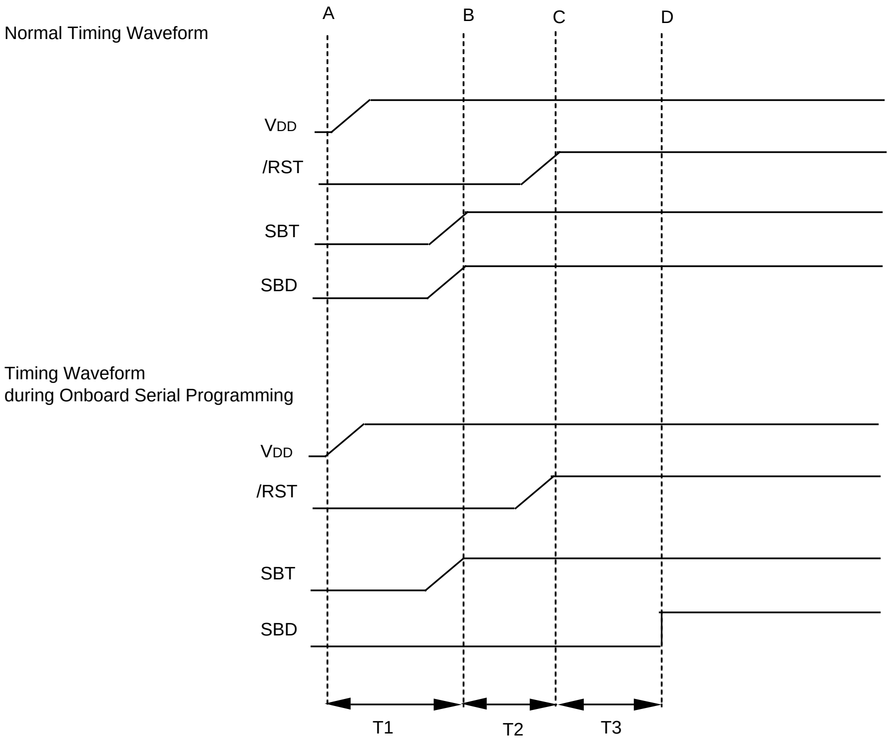

Figure 8-4-6 Setup Timing for Onboard Serial Programming Mode

● Setup Steps

1. Serial writer supplies V_{DD} at Timing A. At this point, output /RST = SBD = Low.
2. The serial writer drives /RST for T2 term from Timing B when SBT goes high from low at ramp-up period. The MN102LF59D is initialized.
3. The serial writer drives SBD for T3 term from Timing C when /RST goes high from low at ramp-up period. This informs that the MN102LF59D is connected to the serial writer.
4. During T3 term, the serial writer makes SBD pin to input low level longer enough than the MN102LF59D stabilization wait time.

● Judgement at Loader

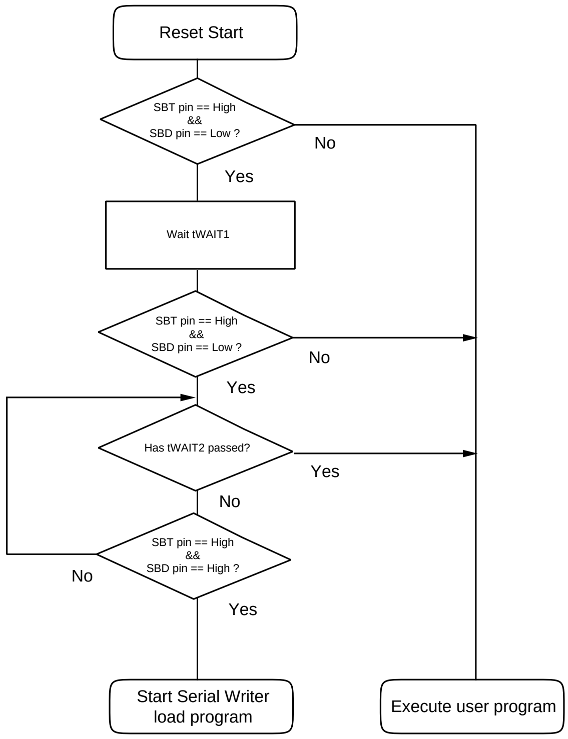

Figure 8-4-7 Determination Flow of Serial Programming Mode

Conditions for Loader Activation

1. When the load program initializes a reset start, SBD = low and SBT = high are must be confirmed.
2. The program waits for tWAIT1.
3. SBD must still be low and SBT high.
4. Wait that both SBD and SBT become high during tWAIT2.

If any above conditions are not met, the program returns to the user program activation.

8-4-9 Branch to the User Program

(1) Branch to Reset Service Routine

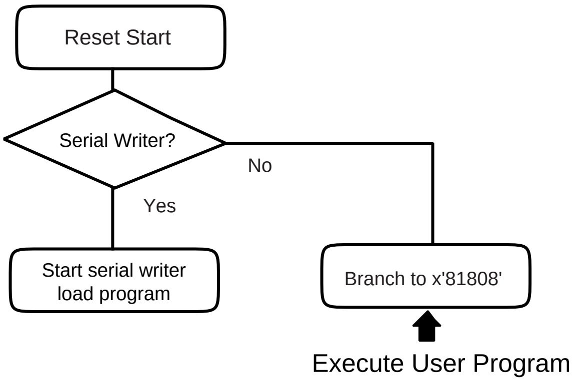

Figure 8-4-8 Reset Service Routine Flow

- At reset start, the serial writer load program is activated only when SBD pin is low.
- The program branches to the user program at address x'81808'.

(2) Branch to Interrupt Service Routine

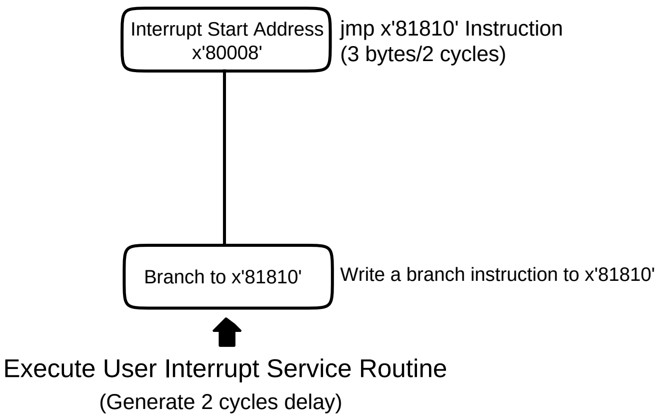

Figure 8-4-9 Interrupt Service Routine Flow

- Only the branch instruction to address x'81810' is written at the interrupt start address (x'80008').

8-4-10 Serial Interface Only for Onboard Serial Programming

■ Features

[Fixed-length Serial Interface]

- Character length	Fixed to 8 bits
- Transmission bit order	Fixed to LSB
- Clock source	External clock
- Maximum transfer rate	5 Mbps (at external 5 MHz oscillation = internal 20-MHz oscillation)
- Error detection	Overrun error
- Buffer	Transmit/reception shared buffer Single transmit buffer, Double reception buffer

■ Data Timing

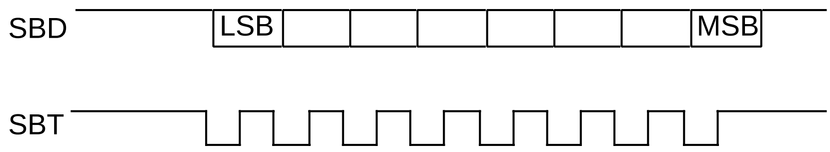

Figure 8-4-10 Data Transfer Timing

The 8-bit serial data is transferred with LSB first bit order.

8-4-11 PROM Writer / Onboard Serial / Programming

■ Programming Flow Diagram

The flash EEPROM program (erase/write) is shown below.

First, flash EEPROM is erased, and User Data Program follows.

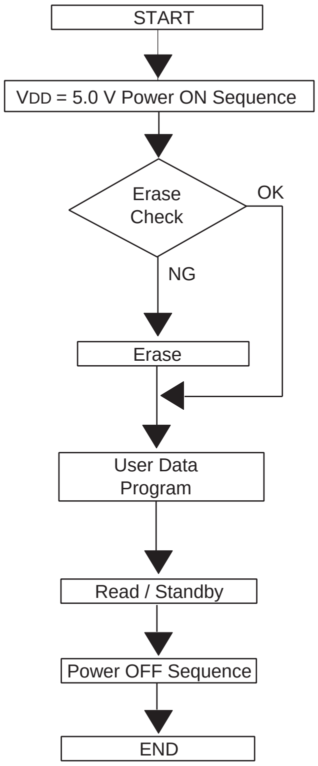

Figure 8-4-11 Programming Flow Chart

When internal flash EEPROM is programmed, be sure to erase it first and after that, write (User Data Program) it. However, some of them are already erased that were shipped from us, so it is possible to write directly. As for others that are unknown where they are from, be sure to erase them first.
Even if the result of “blank check” function that is set on PROM writer or onboard writer is “Pass”, erase level is not satisfying sometimes. In this case, even if a program is normally finished, the programmed data reliability can be doubtful.
Writing in addition the address that has already written is inhibited.

MN102L59D/59C/F59D

LSI User's Manual

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